



N-Channel Enhancement-Mode MOSFET, Logic Level

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



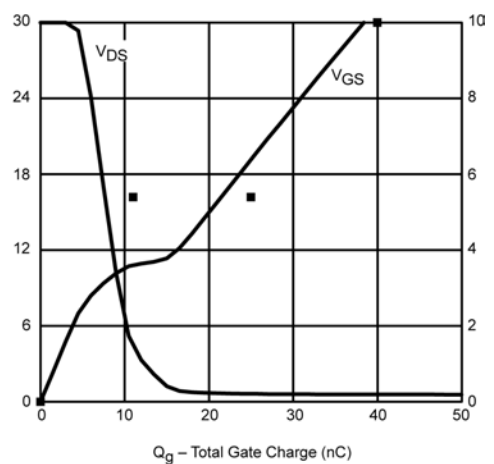
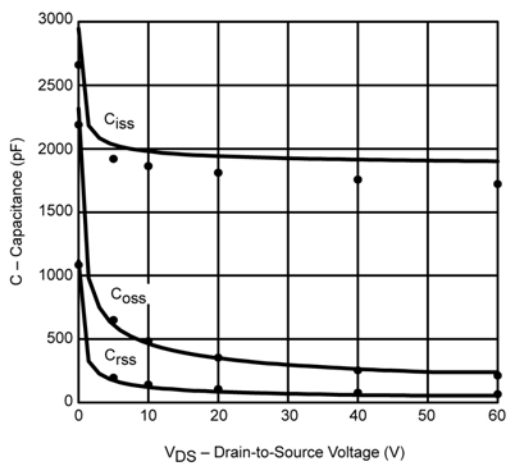
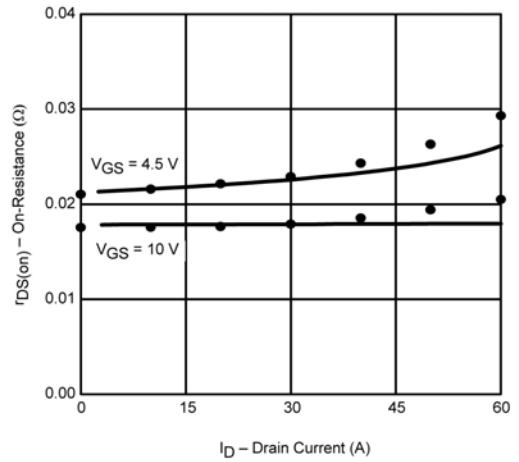
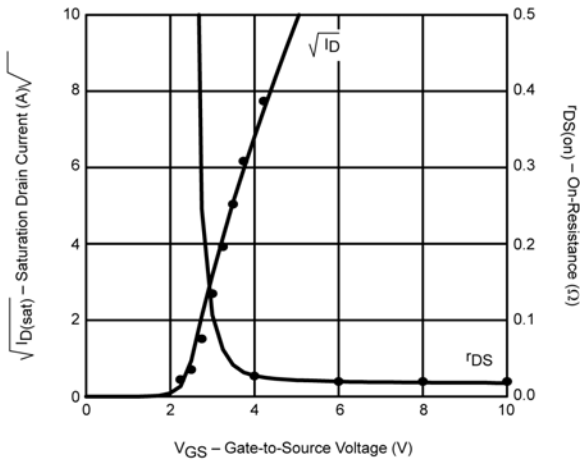
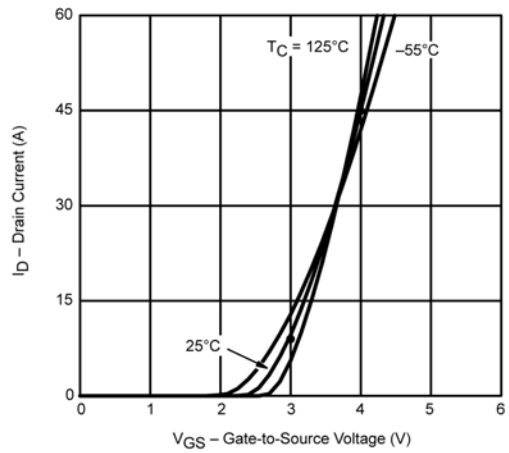
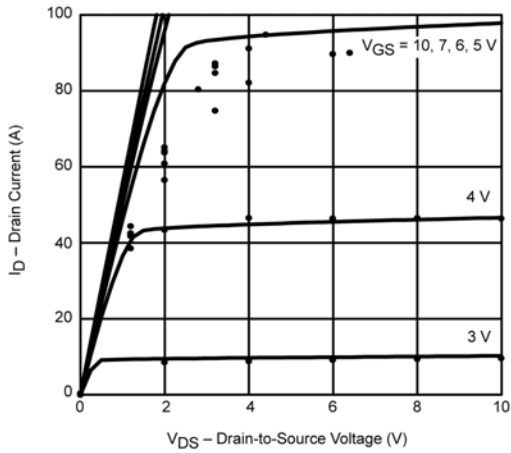
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.6		V
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	268		A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	0.018		Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125°C	0.029		
		V _{GS} = 10 V, I _D = 20 A, T _J = 175°C	0.035		
		V _{GS} = 4.5 V, I _D = 20 A	0.022		
Forward Voltage ^a	V _{SD}	I _F = 34 A, V _{GS} = 0 V	0.90	1	V
Dynamic^b					
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	1933	1800	pF
Output Capacitance	C _{oss}		319	350	
Reverse Transfer Capacitance	C _{rss}		78	100	
Total Gate Charge ^c	Q _g	V _{DS} = 30 V, V _{GS} = 10 V, I _D = 40 A	39	40	nC
Gate-Source Charge ^c	Q _{gs}		9	9	
Gate-Drain Charge ^c	Q _{gd}		10	10	
Turn-On Delay Time ^c	t _{d(on)}	V _{DD} = 30 V, R _L = 0.90 Ω I _D ≅ 34 A, V _{GEN} = 10 V, R _G = 2.5 Ω	11	10	ns
Rise Time ^c	t _r		8	9	
Turn-Off Delay Time ^c	t _{d(off)}		25	28	
Fall Time ^c	t _f		15	7	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 34 A, di/dt = 100 A/μs	31	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



Disclaimer

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