



### N-Channel 60-V (D-S) 175°C MOSFET, Logic Level

#### CHARACTERISTICS

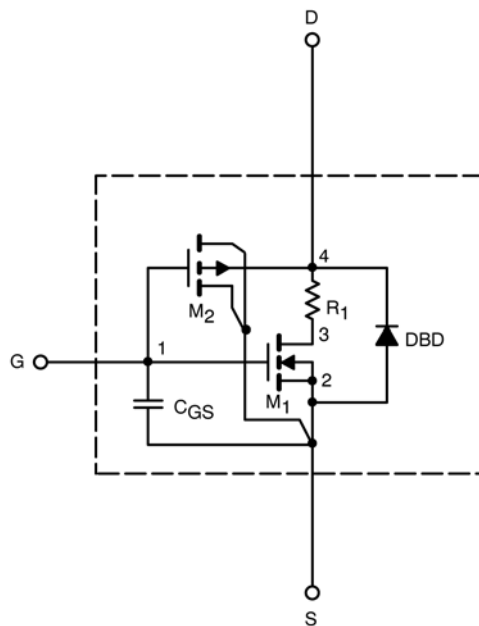
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



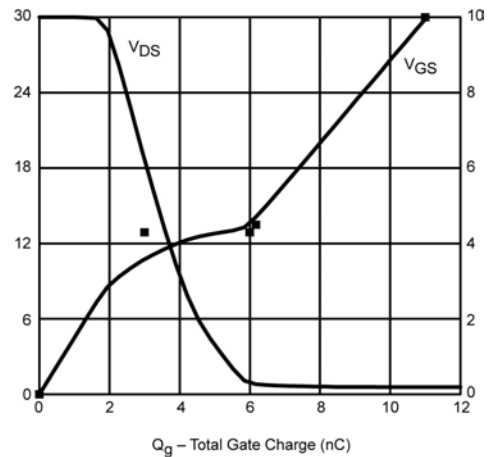
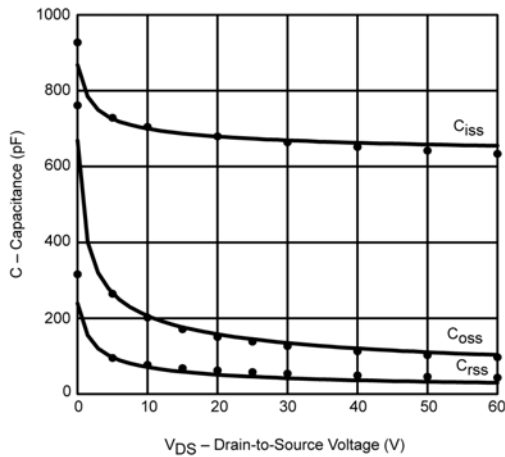
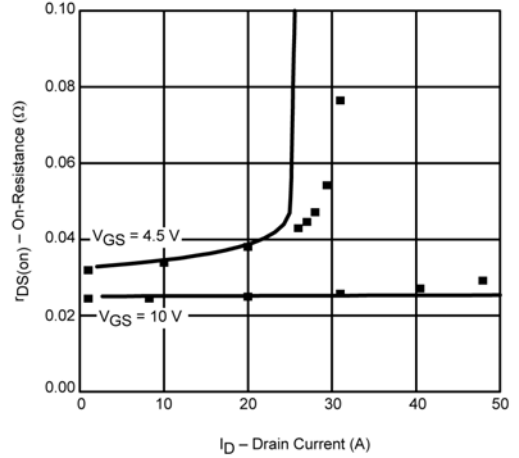
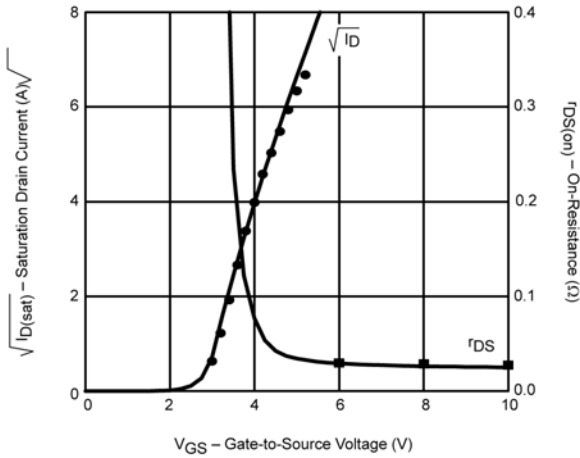
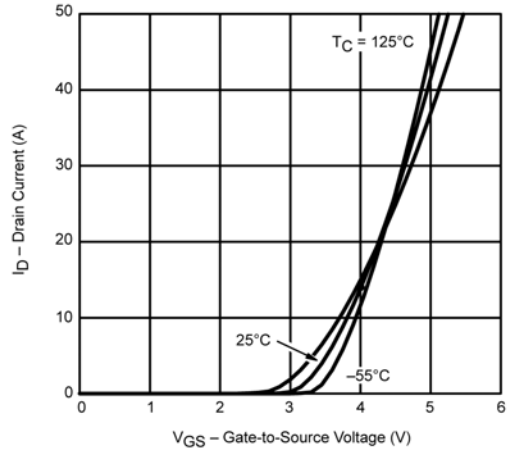
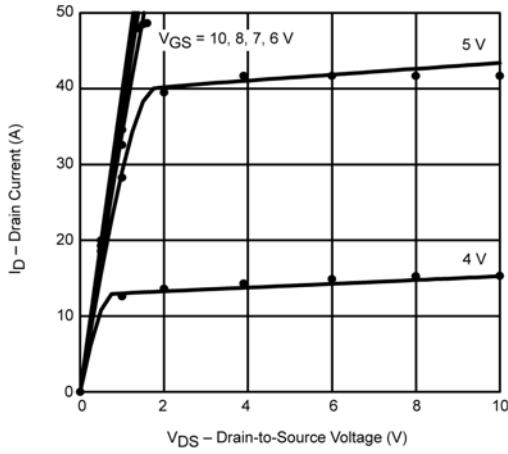
SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
<b>Static</b>					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2.1		V
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	189		A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$	0.025	0.025	$\Omega$
		$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}, T_J = 125^\circ\text{C}$	0.040		
		$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}, T_J = 175^\circ\text{C}$	0.048		
		$V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	0.035	0.037	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 15 \text{ A}, V_{GS} = 0 \text{ V}$	0.88	1	V
<b>Dynamic<sup>b</sup></b>					
Input Capacitance	$C_{iss}$	$V_{GS} = 0 \text{ V}, V_{DS} = 25 \text{ V}, f = 1 \text{ MHz}$	677	670	pF
Output Capacitance	$C_{oss}$		144	140	
Reverse Transfer Capacitance	$C_{rss}$		46	60	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 23 \text{ A}$	11	11	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$		3	3	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$		3	3	
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 30 \text{ V}, R_L = 1.3 \Omega$ $I_D \cong 23 \text{ A}, V_{GEN} = 10 \text{ V}, R_G = 2.5 \Omega$	9	8	ns
Rise Time <sup>c</sup>	$t_r$		8	15	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$		33	30	
Fall Time <sup>c</sup>	$t_f$		10	25	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 34 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	31	48	

**Notes**

- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



## Disclaimer

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