**FUNCTIONAL DESCRIPTION**

The Si4724CY is a high-speed driver designed to operate in high frequency dc-dc switchmode power supplies. It is designed to be used with any single output PWM IC or ASIC to produce a highly efficient synchronous rectifier converter.

Under-voltage protection is provided for the Vdd power supply. The device includes a bootstrap diode, integrated Schottky diode, and fast switching times.

**MODEL DESCRIPTION**

The driver circuit was decomposed into elemental blocks, and then modeled accordingly as per the data sheet and specific topological IC information provided to AEi Systems by Vishay’s engineers.

IsSpice models for the output MOSFETs, bootstrap PNP diode, and the Schottky diode were provided and used in the modeling of the Si4724CY. No efforts were made to improve the models although they were reviewed and comments are shown below.

Using ICAP/4, a SPICE package from AEi Systems, a model of the driver was then created using the modules and a corresponding schematic and netlist was generated.

The model includes the following functionality and features:

- Proper transient response including variations with external components.
- Proper connectivity as per the real-life part
- Output rise and fall times for varying loads
- Under voltage lockout & hysteresis
- Switching times (turn off and propagation delays)
- Schottky behavior
- Bootstrap voltage and diode characteristics
- Logic input voltage thresholds
- Break-before-make reference

Note: The variation of the \( V_{ref} \) and logic input voltage levels with \( V_{DD} \) are not modeled.

The model operation is described as follows:

- \( V_{DD} \) under voltage lockout and threshold is modeled by S2, V10, and R5.
- The \( V_{SVn/Vnc} \), Sync, and \( V_{IN} \) comparisons are handled by B7, B1, and B\(_{n}\), respectively. The logic input threshold value used was 2.3V. This value is static but could be made a function of \( V_{IN} \).
- The RC combinations, R2/C1, R8/C2 and R7/C1 account for the majority of the IO propagation delays and the \( T_{ON}/T_{OFF} \) delay matching.
- The level shifting and the logic functions are modeled by B4 and B5.
- The output FETs have been modeled to provide the appropriate drive performance along with the proper values of \( r_{DSon} \) (values used: G1 n-Channel 0.7 \( \Omega \)/n-Channel 1.5 \( \Omega \), G2 n-Channel 0.5 \( \Omega \)/n-Channel 1 \( \Omega \))

**ASSUMPTIONS**

- Behavior is based on typical values given in the specification sheet for operation at 27 °C.
- Some thermal variations are modeled including some FET related parameters and the propagation delay and are represented in the subcircuit.
- The SPICE syntax used is compatible with Intusoft ICAP/4. A PSpice version of the subcircuit is also provided.
SPICE Device Model Si4724CY
Vishay Siliconix

IS SPICE 4 NETLIST

*================================================================================================*
* Vishay Si4724CY
* This model was developed for Vishay by:
* AEI Systems, LLC
* 5777 W. Century Blvd. Suite 876
* Los Angeles, California 90045
* Copyright 2003, all rights reserved.
* This model is subject to change without notice.
* Users may not directly or indirectly re-sell or re-distribute this model.
* For more information regarding modeling services, model libraries and simulation products, please call AEI Systems at (310) 216-1144, or contact AEI by email: info@aeng.com. http://www.AENG.com
* Revision: 6/3/02, version 1.1
* Revision: 1/28/04, version 1.1
* Updated driver voltages and VTO to reduce IC current draw.
* Note, do not trust spice to have accurate currents.
*
**********
* SRC=Si4724CY;Si4724CY;Drivers;Power Mosfet;Synchronous
* SYM=Si4724CY
.SUBCKT Si4724CY VDD Vin Sync Gnd Boot D1 S1 D2 S2
                    VDD Vin Sync Gnd Boot D1 S1 D2 S2
# alias bbm v(bbm)
# alias g1 v(g1)
# alias in v(in)
# alias syncin v(18)
# alias in2 v(in2)
# alias in3 v(in3)
# alias vout v(vout)
# alias vboot v(boot)
# alias vootch v(s1)
# alias vdduvlo v(vdduvlo)
# alias g2 v(g2)
V10 Vdd 0 DC=5
B1 15 gnd V=5
Q1 Boot Boot VDDABSD
.MODEL SIDVBAD PNP BF=1.2465489 BR=0.0743382
  + CJC=2.48725E-10 CE=1.49509E-10 EG=1.32 FC=0.05
  + KF=10.675593 KF=100.984516E-8 IS=5.828556E-18
  + IS=5.929013E-14 IS=1.45909E-10 EG=1.32 FC=0.05
  + MJE=0.3267463 NC=1.0479867 NF=0.9018194
  + VJE=0.803 XTI=3.4 XTI=0.5
B5 8 G1 V=V(VDDUVLO) > 1 ? V(VDDUVLO) > 4 ? 5 : 0
R8 11 8 35
C3 G1 11 30p
X3 D2 G2 S2 SIFETADY ( )
R2 14 16 200
C1 16 gnd 100p
B2 1n2 gnd V(VDDUVLO) > 4 ? 5 : 0
R10 15 18 170
C5 18 gnd 200p

Table 1: IsSpice4 Subcircuit Netlist
MODEL VERIFICATION

The test circuit described in the data sheet as Figure 4 was created using ICAP/4, and shown in figure 2. The model was tested as per the manufacturer’s datasheet using component values provided by Vishay.

The results of the simulation performance for various model aspects are shown in the following figures.

Note: The configuration in Figure 1 and this schematic were used for propagation delay, delay matching, and rise/fall time tests. Capacitor ESR/ESL and leakage were estimated.
Figure 2: Single input pulse simulation results. Note the dip in Vswitch (green waveform)

Figure 3: Delta t1-2 Propagation delay simulation results (falling edge of IN)
Figure 4: Delta t2-1 Propagation delay simulation results (rising edge of IN)

Figure 5: Startup simulation shows VOUT (top graph) and VOUT, Vswitch (S1/D1), and IN (bottom graph)
Figure 6: Response of the G1 and G2 signals for Sync pulse

Figure 7: Turn-on/Turn-off and hysteresis for V_{DD}
CONCLUSIONS

The model of the SI4724CY driver correlates very well with the manufacturer’s datasheet and meets all of the items listed in the Statement of Work (SOW). This data should be verified against actual hardware for further confirmation.

The output voltage (1.4 V) is somewhat less than the 1.6 V that should be achieved with an input pulse width of 545us (0.545u/4u). The reason for this is unknown.

The variation of the V\text{ref} and logic input voltage levels with V\text{DD} are not modeled but could be added.

The reader is referred to three references on this topic.

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