



# N-Channel 30-V (D-S) MOSFET

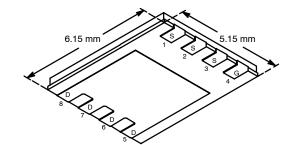
PRODUCT SUMMARY						
V <sub>DS</sub> (V)	$r_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ)			
30	0.00325 @ V <sub>GS</sub> = 10 V	30	36			
	0.0042 @ V <sub>GS</sub> = 4.5 V	27	30			

# FEATURES

- Ultra-Low On-Resistance Using High Density TrenchFET® Gen II Power MOSFET Technology
- Q<sub>g</sub> Optimized
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100% R<sub>g</sub> Tested

### **APPLICATIONS**

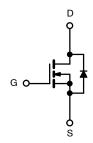
- Low-Side DC/DC Conversion
  - Notebook
  - Server
  - Workstation
- Synchronous Rectifier, POL



PowerPAK SO-8

Bottom View

Ordering Information: Si7336DP-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter		Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage		V <sub>DS</sub>	30		٧	
Gate-Source Voltage		V <sub>GS</sub>	±20			
0.11. D.: 017. 150000	T <sub>A</sub> = 25°C	l <sub>D</sub>	30	18		
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	T <sub>A</sub> = 70°C		25	15		
Pulsed Drain Current (10 μs Pulse Width)		I <sub>DM</sub>	70		Α	
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	4.5	1.8		
Avalanche Current	L = 1.0 mH	I <sub>AS</sub>	50			
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25°C	Б	5.4	1.9	w	
	T <sub>A</sub> = 70°C	P <sub>D</sub>	3.4	1.2		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to 150		°C	

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
	t ≤ 10 sec	R <sub>thJA</sub>	18	23		
Maximum Junction-to-Ambient <sup>a</sup>	Steady State		50	65	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R <sub>thJC</sub>	1.0	1.5		

#### Notes

a. Surface Mounted on 1" x 1" FR4 Board.

# **Vishay Siliconix**



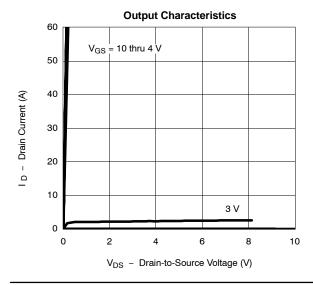
Parameter	Symbol	Test Condition	Min	Тур	Max	Unit
Static						
Gate Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.0		3.0	V
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			1 5	μΑ
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS} = 10$ V, $I_D = 25$ A $V_{GS} = 4.5$ V, $I_D = 19$ A		0.0026	0.00325	Ω
Forward Transconductancea	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 25 A		110		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.9 A, V <sub>GS</sub> = 0 V		0.72	1.1	V
Dynamic <sup>b</sup>	1		<b>"</b>	·I	I	
Input Capacitance	C <sub>iss</sub>			5600		pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 15 \text{ V}, \ V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		860		
Reverse Transfer Capacitance	C <sub>rss</sub>			415		
Total Gate Charge	Qg			36	50	nC
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS}$ = 15 V, $V_{GS}$ = 4.5 V, $I_D$ = 20 A		18		
Gate-Drain Charge	Q <sub>gd</sub>			10		
Gate Resistance	$R_g$		0.8	1.3	2.0	Ω
Turn-On Delay Time	t <sub>d(on)</sub>			24	35	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 15 V, $R_L$ = 15 $\Omega$		16	25	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$		90	140	ns
Fall Time	t <sub>f</sub>			32	50	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 2.9 A, di/dt = 100 A/μs		45	70	ĺ

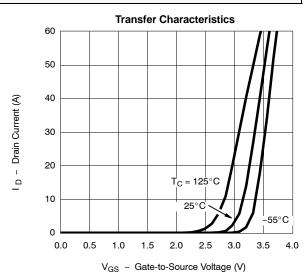
### Notes

- a. Pulse test; pulse width  $\leq~300~\mu\text{s},$  duty cycle  $\leq~2\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



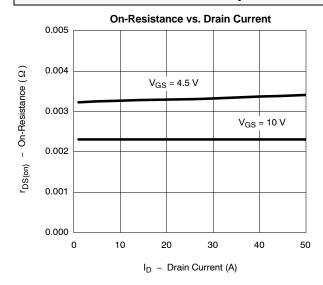


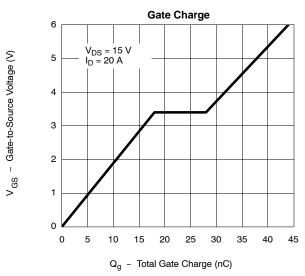


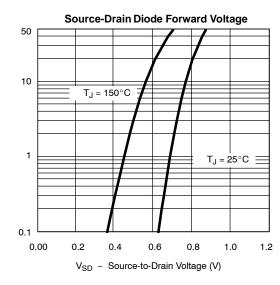


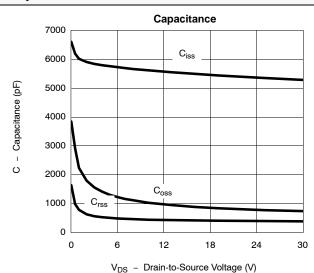


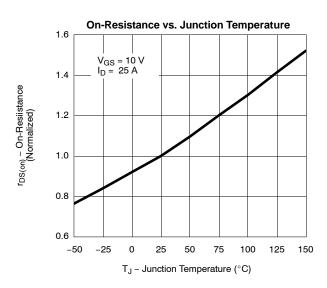
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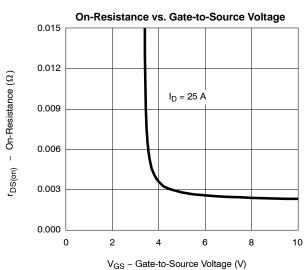












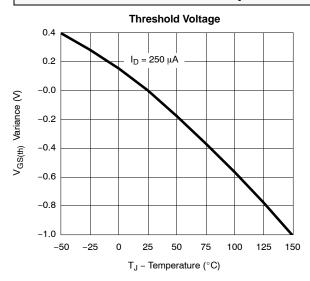
- Source Current (A)

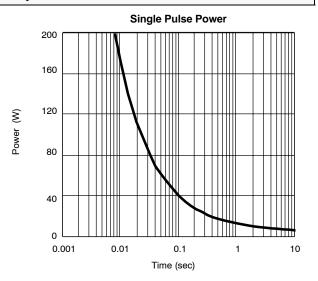
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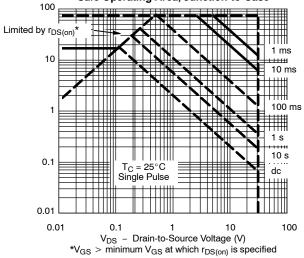


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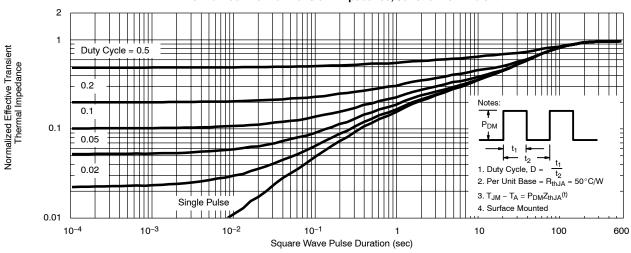




### Safe Operating Area, Junction-to-Case



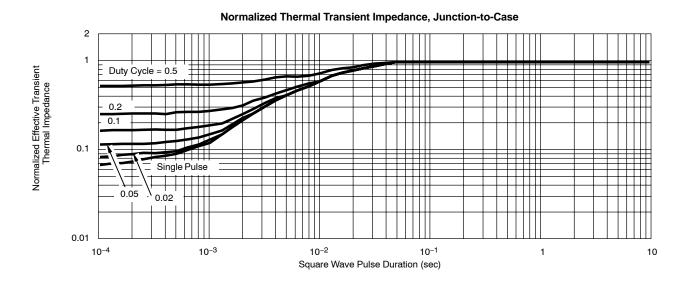
### Normalized Thermal Transient Impedance, Junction-to-Ambient







### TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?72415">http://www.vishay.com/ppg?72415</a>.



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