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N-Channel 40 V (D-S) 175 °C MOSFET

DESCRIPTION

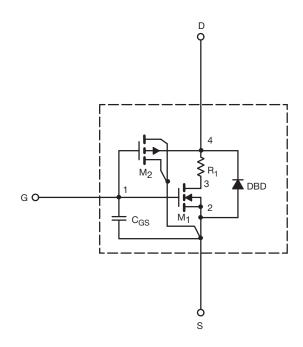
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPICE Device Model SUM70N04-07L

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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1.9	-	V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	784	-	Α
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}$	0.0060	0.0060	Ω
		$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}, T_J = 125 ^{\circ}\text{C}$	0.0096	-	
		$V_{GS} = 10 \text{ V}, I_D = 30 \text{ A}, T_J = 175 ^{\circ}\text{C}$	0.0115	-	
		V _{GS} = 4.5 V, I _D = 10 A	0.0083	0.0085	
Forward Transconductancea	9fs	$V_{DS} = 15 \text{ V}, I_D = 30 \text{ A}$	59	57	S
Diode Forward Voltage	V_{SD}	I _S = 30 A, V _{GS} = 0 V	0.9	1	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	2784	2800	pF
Output Capacitance	Coss		328	320	
Reverse Transfer Capacitance	C _{rss}		188	190	
Total Gate Charge	Qg	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 50 A	50	50	nC
Gate-Source Charge	Q_{gs}		10	10	
Gate-Drain Charge	Q _{gd}		10	10	
Turn-On Delay Time	t _{d(on)}	$V_{DD} = 20 \text{ V}, \text{ R}_{L} = 0.4 \Omega$ $I_{D} = 50 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 2.5 \Omega$	21	11	ns
Rise Time	t _r		15	20	
Turn-Off Delay Time	t _{d(off)}		29	40	
Fall Time	t _f		23	15	

Notes

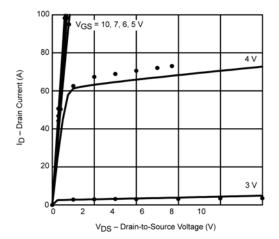
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

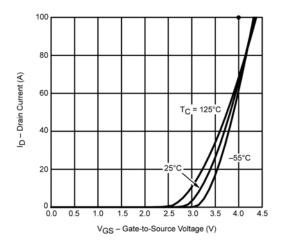


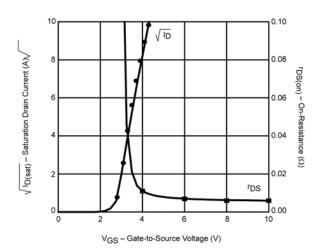
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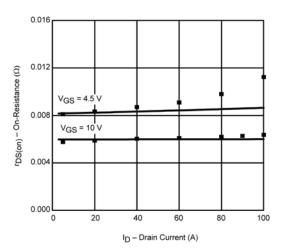
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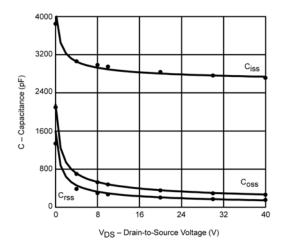
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25$ °C, unless otherwise noted)

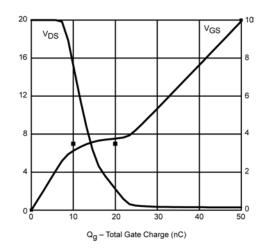












Note

• Dots and squares represent measured data.



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