



### Complementary 30-V (D-S) MOSFET

#### CHARACTERISTICS

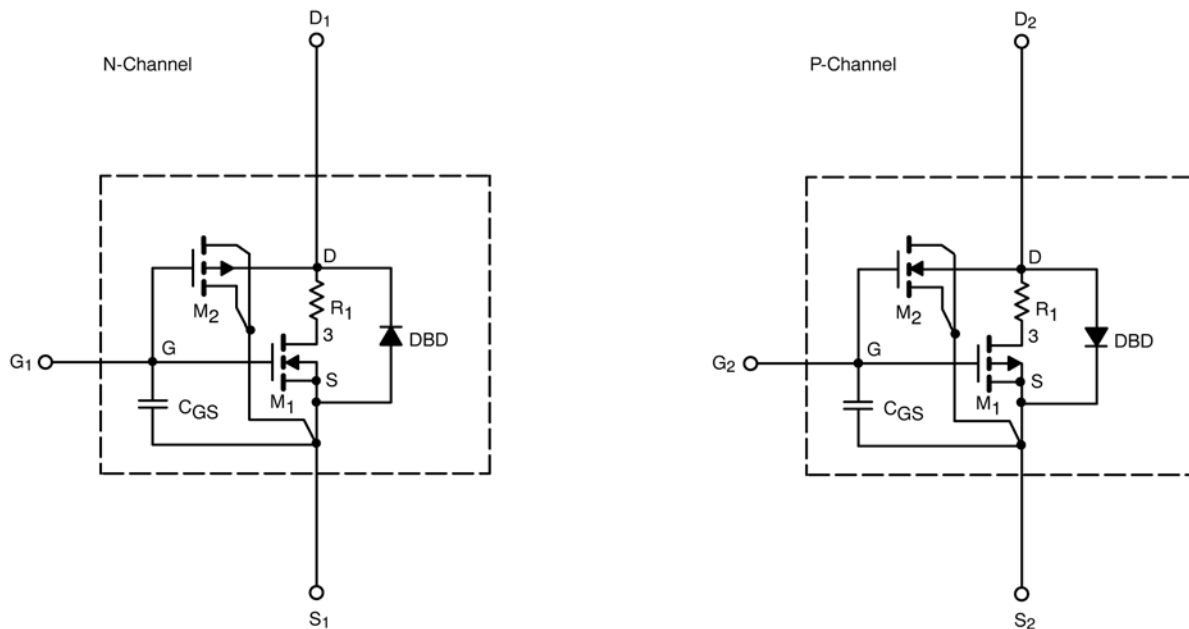
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition		Simulated Data	Measured Data	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	2.6		V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	2.1		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ -5 V, V <sub>GS</sub> = -10 V	P-Ch	105		A
		V <sub>DS</sub> ≤ 5 V, V <sub>GS</sub> = 10 V	N-Ch	171		
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -6.4 A	P-Ch	0.041	0.041	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.7 A	N-Ch	0.027	0.028	
		V <sub>GS</sub> = -6 V, I <sub>D</sub> = -5.3 A	P-Ch	0.055	0.055	
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.5 A	N-Ch	0.039	0.040	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -6.4 A	P-Ch	11	13	S
		V <sub>DS</sub> = 15 V, I <sub>D</sub> = 7.7 A	N-Ch	15	15	
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -1.7 A, V <sub>GS</sub> = 0 V	P-Ch	0.85	0.80	V
		I <sub>S</sub> = 1.7 A, V <sub>GS</sub> = 0 V	N-Ch	0.80	-0.80	
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	P-Channel V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -6.4 A  N-Channel V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 7.7 A	P-Ch	9	12.5	nC
			N-Ch	8.6	9	
Gate-Source Charge	Q <sub>gs</sub>		P-Ch	2.5	2.5	
			N-Ch	2	2	
Gate-Source Charge	Q <sub>gs</sub>	P-Ch	3.6	3.6	ns	
		N-Ch	1.3	1.3		
Turn-On Delay Time	t <sub>d(on)</sub>	P-Channel V <sub>DD</sub> = -15 V, R <sub>L</sub> = 5 Ω I <sub>D</sub> ≅ -3 A, V <sub>GEN</sub> = -10 V, R <sub>G</sub> = 1 Ω  N-Channel V <sub>DD</sub> = 15 V, R <sub>L</sub> = 5 Ω I <sub>D</sub> ≅ 3 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 1 Ω	P-Ch	18	10	
Rise Time	t <sub>r</sub>		N-Ch	9	10	
			P-Ch	12	20	
Turn-Off Delay Time	t <sub>d(off)</sub>		N-Ch	5	15	
			P-Ch	11	25	
Fall Time	t <sub>f</sub>		N-Ch	59	20	
			P-Ch	7	30	
				N-Ch	8	10

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

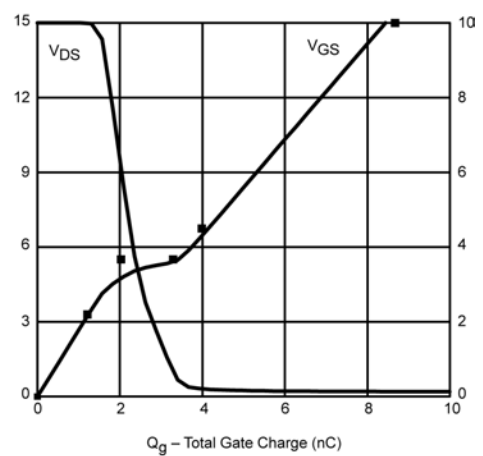
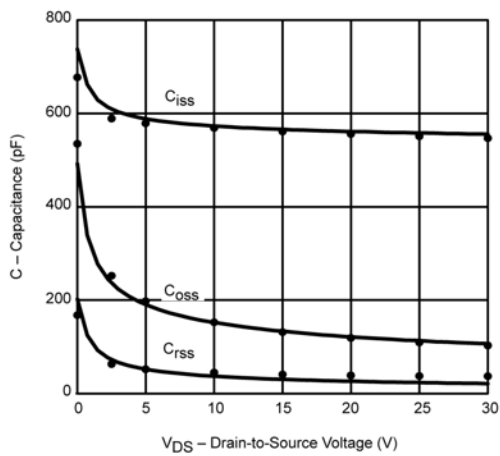
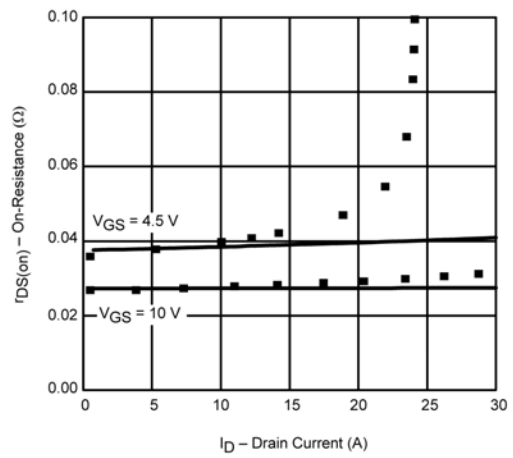
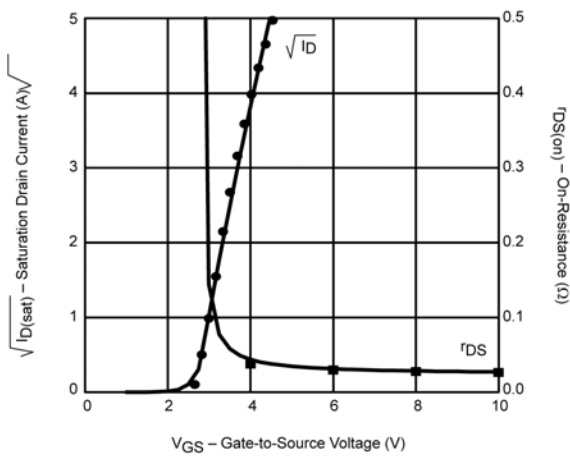
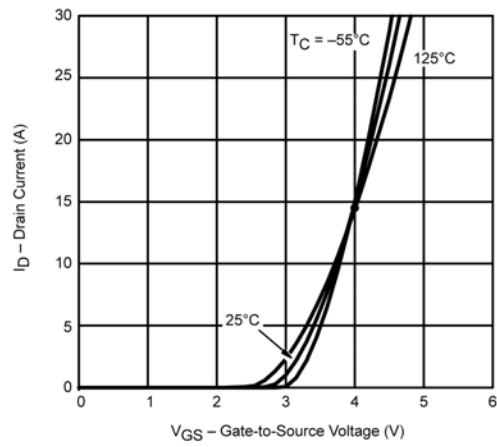
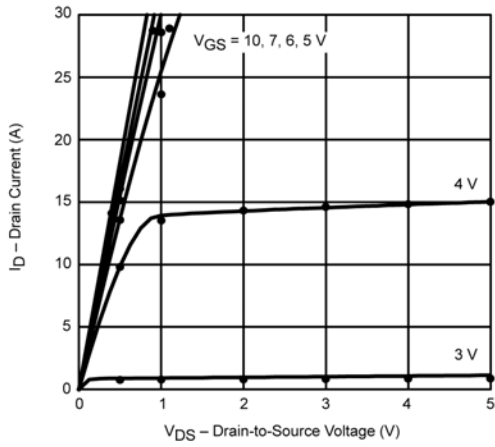


# SPICE Device Model Si7501DN

## Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

### N-Channel MOSFET



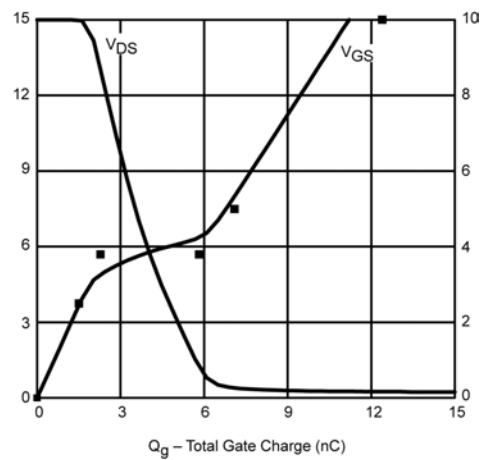
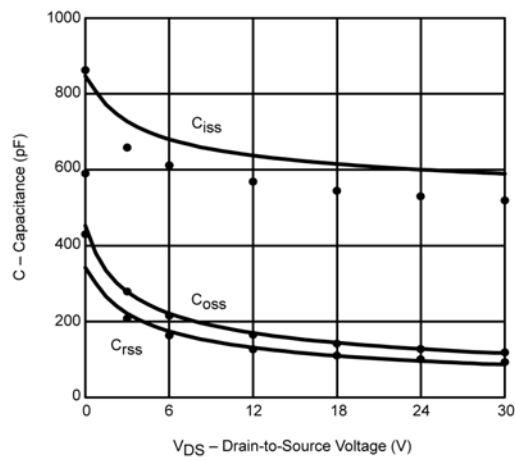
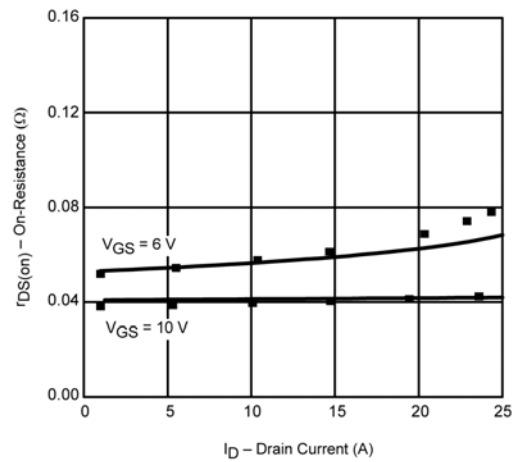
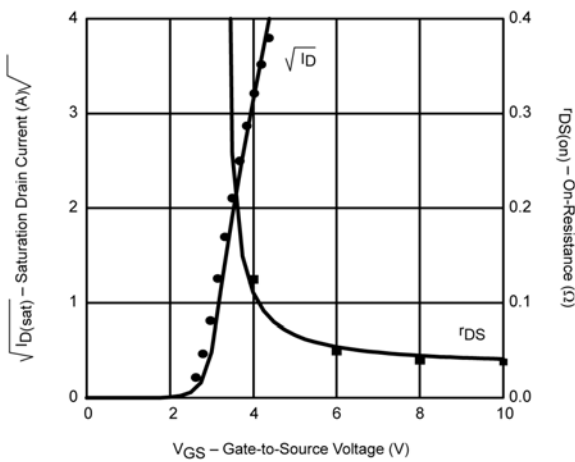
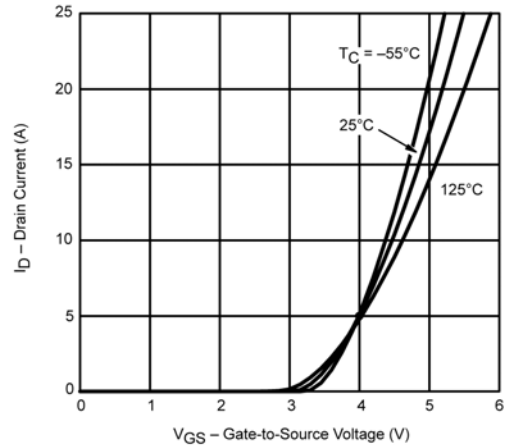
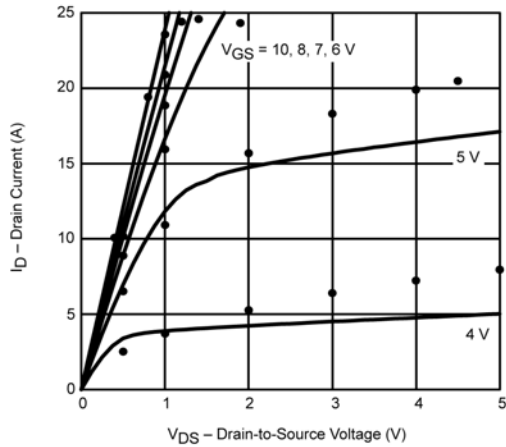
Note: Dots and squares represent measured data.

# SPICE Device Model Si7501DN

## Vishay Siliconix



### P-Channel MOSFET



Note: Dots and squares represent measured data.



## Disclaimer

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