

P-Channel 30 V (D-S) 175 °C MOSFET

DESCRIPTION

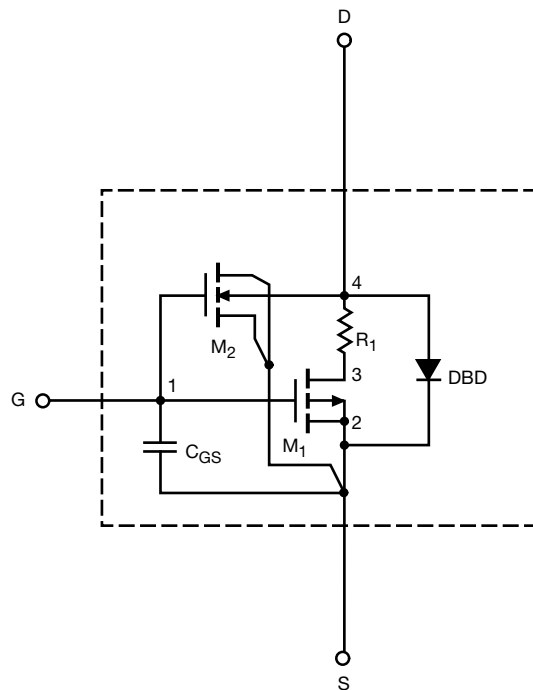
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



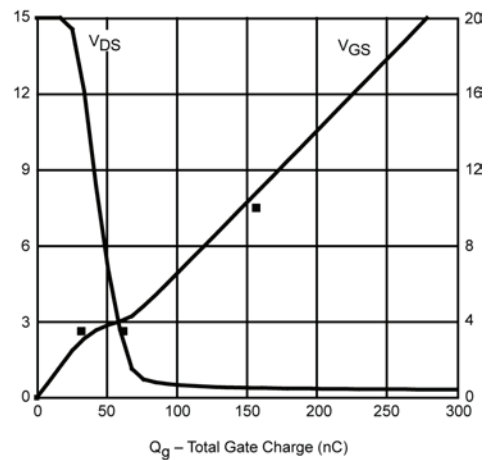
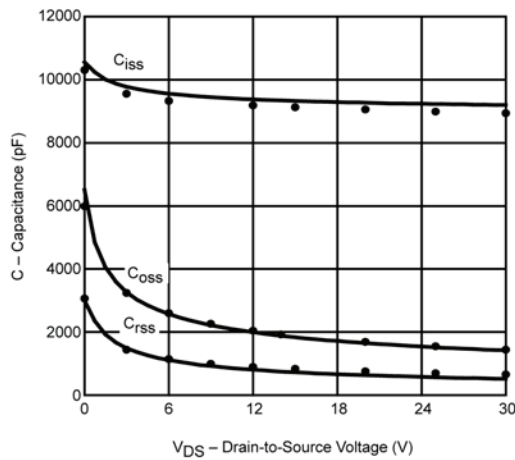
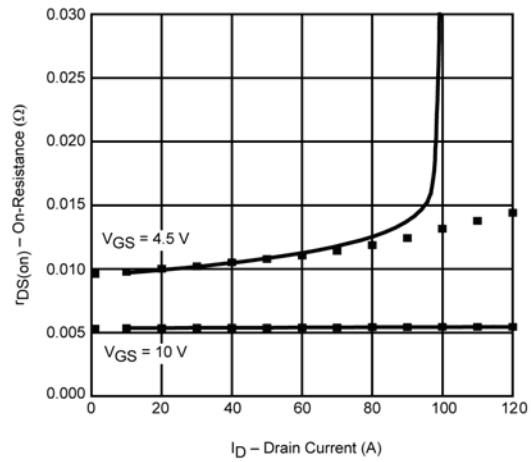
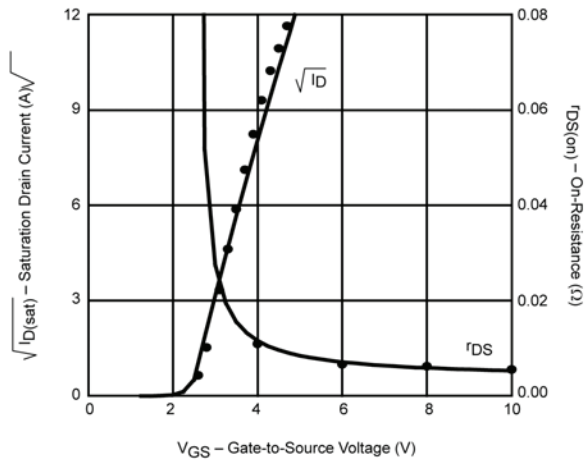
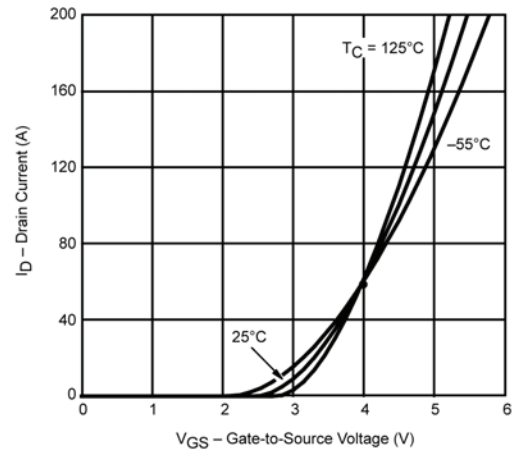
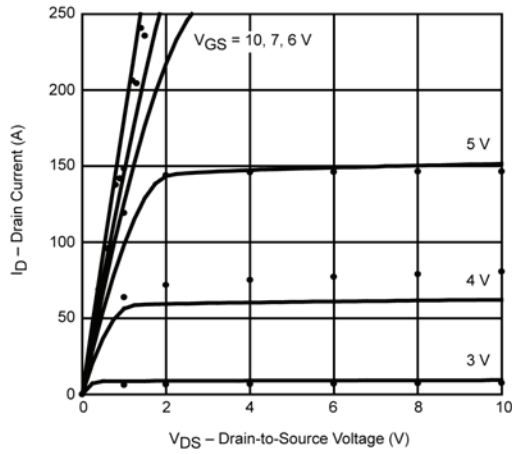
SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	1.8	-	V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\text{ V}, V_{GS} = -10\text{ V}$	772	-	A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -30\text{ A}$	0.0054	0.0055	Ω
		$V_{GS} = -10\text{ V}, I_D = -30\text{ A}, T_J = 125\text{ }^\circ\text{C}$	0.0079	-	
		$V_{GS} = -10\text{ V}, I_D = -30\text{ A}, T_J = 175\text{ }^\circ\text{C}$	0.0093	-	
		$V_{GS} = -4.5\text{ V}, I_D = -20\text{ A}$	0.009	0.008	
Diode Forward Voltage ^a	V_{SD}	$I_F = -75\text{ A}, V_{GS} = 0\text{ V}$	0.92	1.2	V
Dynamic ^b					
Input Capacitance	C_{iss}	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	9242	9000	pF
Output Capacitance	C_{oss}		1533	1565	
Reverse Transfer Capacitance	C_{rss}		578	715	
Total Gate Charge ^c	Q_g	$V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -75\text{ A}$	153	160	nC
Gate-Source Charge ^c	Q_{gs}		32	32	
Gate-Drain Charge ^c	Q_{gd}		30	30	
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 0.2\text{ }\Omega$ $I_D = -75\text{ A}, V_{GEN} = -10\text{ V}, R_g = 2.5\text{ }\Omega$	137	25	ns
Rise Time ^c	t_r		107	225	
Turn-Off Delay Time ^c	$t_{d(off)}$		153	150	
Fall Time ^c	t_f		56	210	

Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.

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