

SPICE Device Model Si8902EDB Vishay Siliconix

Bi-Directional N-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

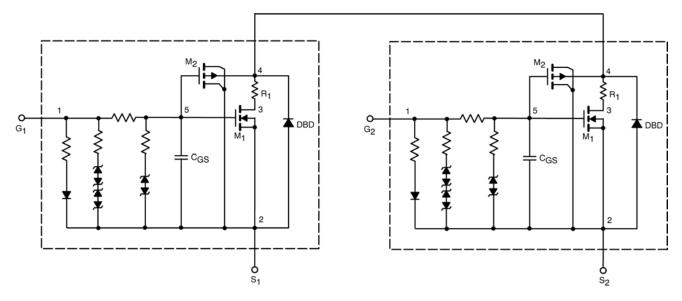
- · Apply for both Linear and Switching Application
- Accurate over the –55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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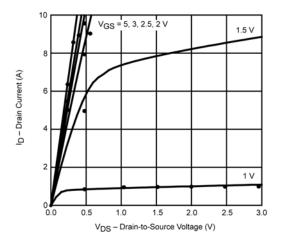
SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static	-		_		
Gate Threshold Voltage	$V_{GS(th)}$	$V_{sS} = V_{GS}, I_D = 250 \mu A$	0.51		V
On-State Drain Current ^a	I _{ss(on)}	$V_{sS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	109		Α
Drain-Source On-State Resistance ^a		V_{GS} = 4.5 V, I_{ss} = 1 A	0.038	0.038	Ω
	R _{sS(on)}	$V_{GS} = 3.7 \text{ V}, I_{ss} = 1 \text{ A}$	0.040	0.041	
		$V_{GS} = 2.5 \text{ V}, I_{ss} = 1 \text{ A}$	0.046	0.048	
		V_{GS} = 1.8 V, I_{ss} = 1 A	0.057	0.060	
Forward Transconductance ^a	g _{fs}	V _{sS} = 10 V, I _{SS} = 1 A	11	20	S
Dynamic ^b					
Turn-On Delay Time	t _{d(on)}	V_{ss} = 10 V, R_L = 10 Ω $I_{ss} \cong$ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω	4	1	μ s
Rise Time	t _r		2	3	
Turn-Off Delay Time	$t_{d(off)}$		7	17	
Fall Time	t _f		4	10	

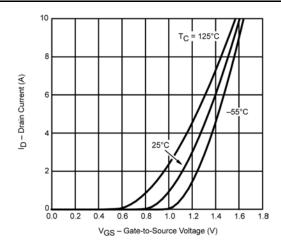
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.

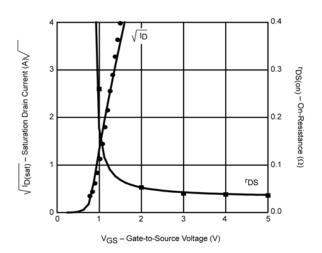


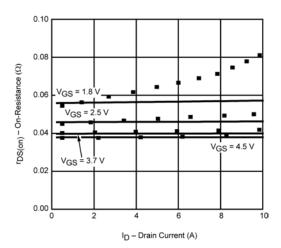
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COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)











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