

N-Channel 60 V (D-S) 175 °C MOSFET

DESCRIPTION

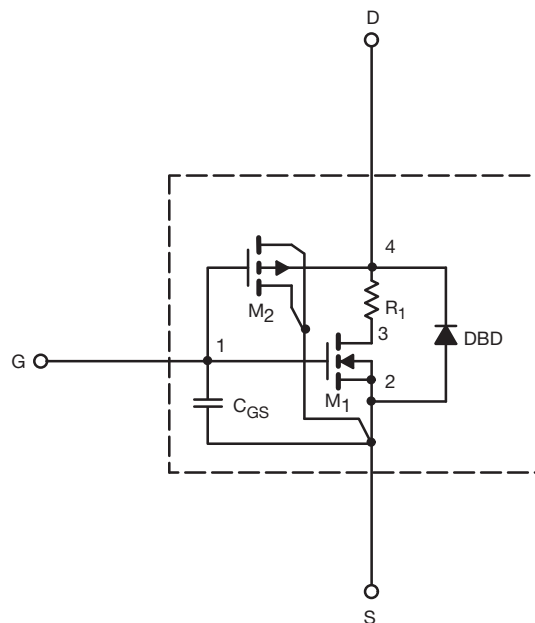
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

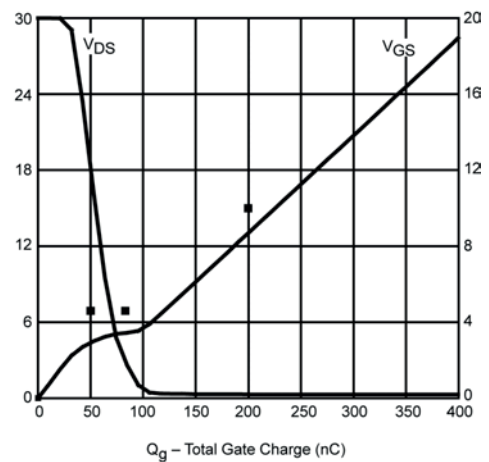
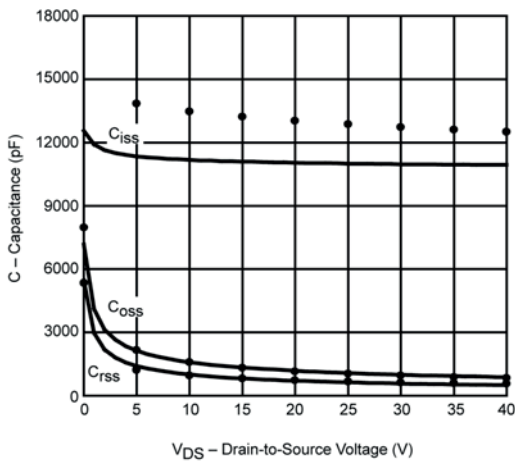
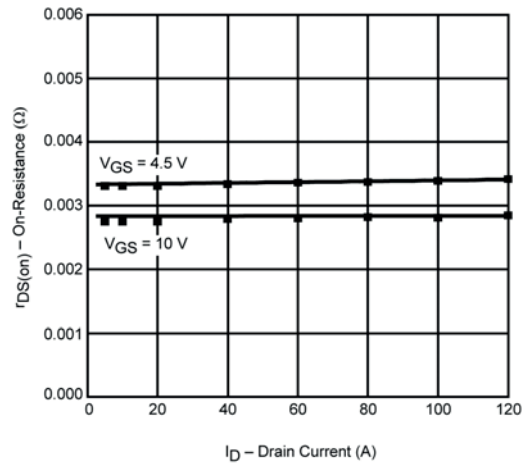
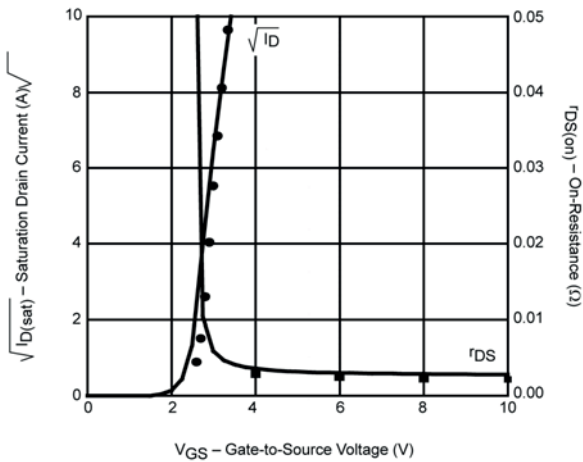
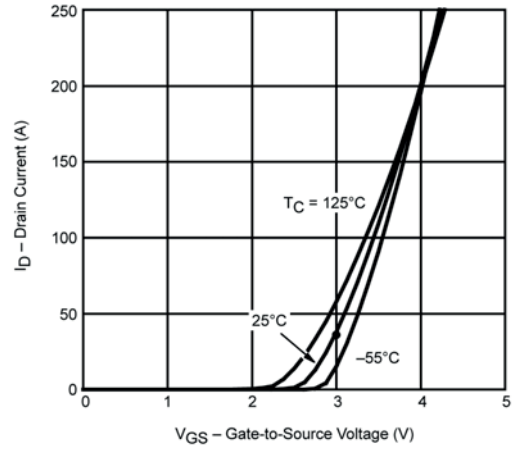
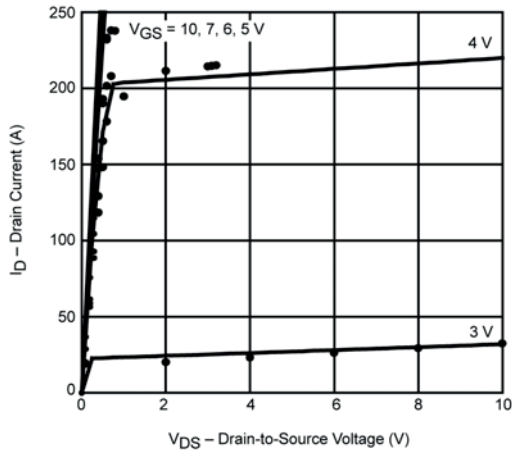
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
|---|---------------------|--|----------------|---------------|------|
| Static | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 1.5 | - | V |
| On-State Drain Current ^a | I _{D(on)} | V _{DS} = 5 V, V _{GS} = 10 V | 1640 | - | A |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = 10 V, I _D = 30 A | 0.0028 | 0.0028 | Ω |
| | | V _{GS} = 10 V, I _D = 30 A, T _J = 125 °C | 0.0041 | - | |
| | | V _{GS} = 10 V, I _D = 30 A, T _J = 175 °C | 0.0047 | - | |
| | | V _{GS} = 4.5 V, I _D = 20 A | 0.0036 | 0.0033 | |
| Diode Forward Voltage | V _{SD} | I _F = 90 A, V _{GS} = 0 V | 0.90 | 1 | V |
| Dynamic^b | | | | | |
| Input Capacitance | C _{iss} | V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz | 11 010 | 12 900 | pF |
| Output Capacitance | C _{oss} | | 1088 | 1060 | |
| Reverse Transfer Capacitance | C _{rss} | | 645 | 70 | |
| Total Gate Charge ^c | Q _g | V _{DS} = 30 V, V _{GS} = 10 V, I _D = 110 A | 224 | 200 | nC |
| Gate-Source Charge ^c | Q _{gs} | | 50 | 50 | |
| Gate-Drain Charge ^c | Q _{gd} | | 33 | 33 | |

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.



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