SPICE Device Model Si7439DP



Vishay Siliconix

P-Channel 150 V (D-S) MOSFET

DESCRIPTION

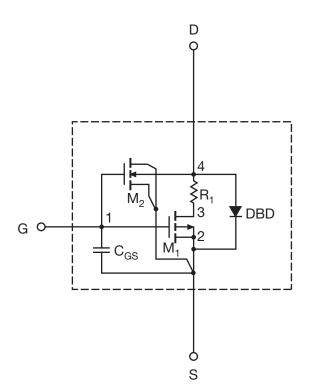
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.





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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$	2.9	-	V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = -10 \text{ V}, \text{ V}_{GS} = -10 \text{ V}$	66	-	А
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -10 \text{ V}, \text{ I}_{D} = -5.2 \text{ A}$	0.075	0.073	Ω
		$V_{GS} = -6 V, I_D = -5 A$	0.080	0.077	
Forward Transconductance ^a	9 _{fs}	$V_{DS} = -15 \text{ V}, \text{ I}_{D} = -5.2 \text{ A}$	17	19	S
Diode Forward Voltage	V _{SD}	I _S = - 4.2 A, V _{DS} = 0 V	- 0.84	- 0.78	V
Dynamic ^b					
Total Gate Charge	Qg	V_{DS} = - 75 V, V_{GS} = - 10 V, I_D = - 5.2 A	89	88	nC
Gate-Source Charge	Q _{gs}		17.5	17.5	
Gate-Drain Charge	Q _{gd}		26.5	26.5	

Notes

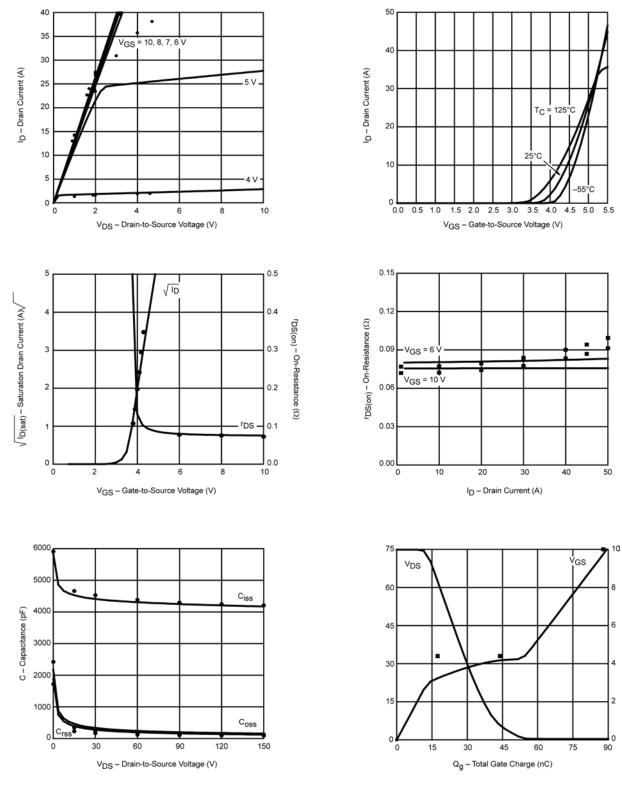
a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data.

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