Dual N-Channel 30-V (D-S) MOSFET with Schottky Diode

CHARACTERISTICS

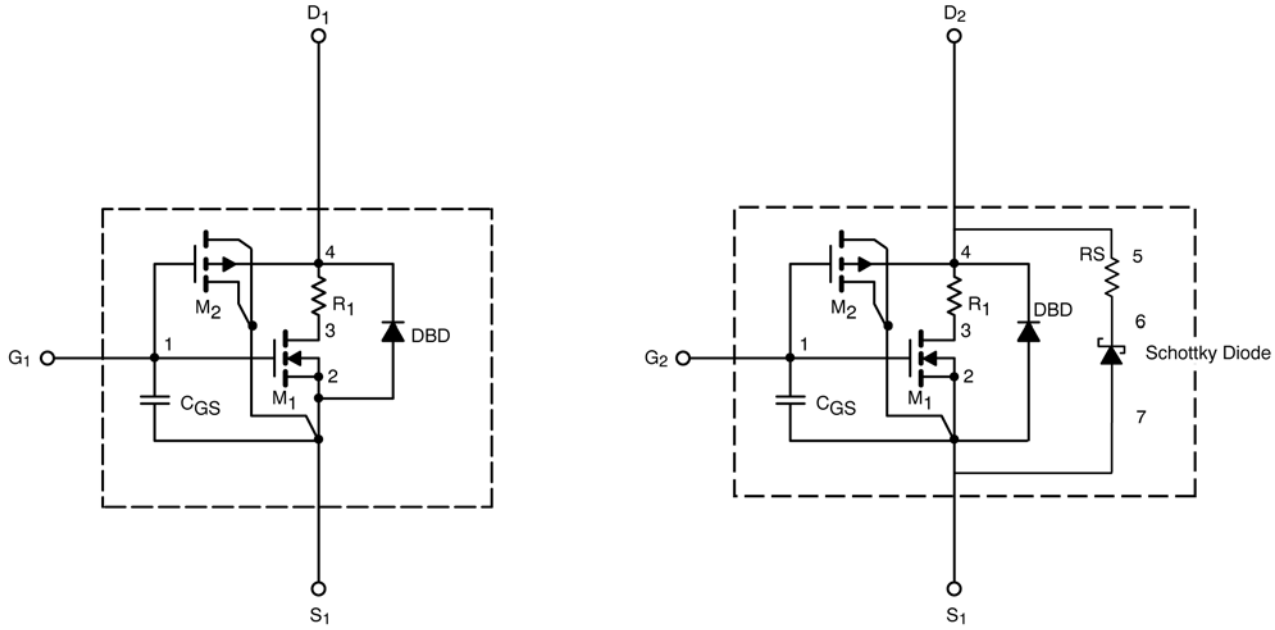
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

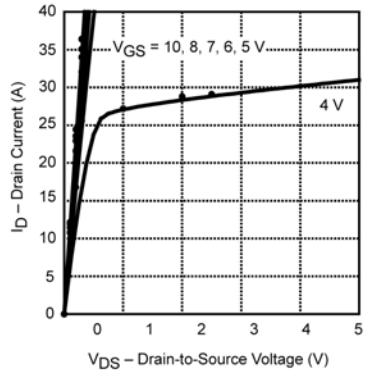
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Conditions**		**Simulated Data**	**Measured Data**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	Ch-1	2.1		V
			Ch-2	1.8		
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	Ch-1	490		A
			Ch-2	725		
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 10 A	Ch-1	0.009	0.009	Ω
		V_{GS} = 10 V, I_D = 14 A	Ch-2	0.0066	0.0065	
		V_{GS} = 4.5 V, I_D = 8.2 A	Ch-1	0.013	0.013	
		V_{GS} = 4.5 V, I_D = 13 A	Ch-2	0.0076	0.0075	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 10 A	Ch-1	31	30	S
		V_{DS} = 15 V, I_D = 14 A	Ch-2	43	60	
Diode Forward Voltage[a]	V_{SD}	I_S = 1.8 A, V_{GS} = 0 V	Ch-1	0.81	0.76	V
		I_S = 2.73 A, V_{GS} = 0 V	Ch-2	0.47	0.485	
Dynamic[a]						
Total Gate Charge	Q_g	Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 10 A Channel-2 V_{DS} = 15 V, V_{GS} = 4. 5V, I_D = 14 A	Ch-1	13	12	nC
			Ch-2	21	19	
Gate-Source Charge	Q_{gs}		Ch-1	5.3	5.3	
			Ch-2	10	10	
Gate-Drain Charge	Q_{gd}		Ch-1	4.3	4.3	
			Ch-2	5	5	

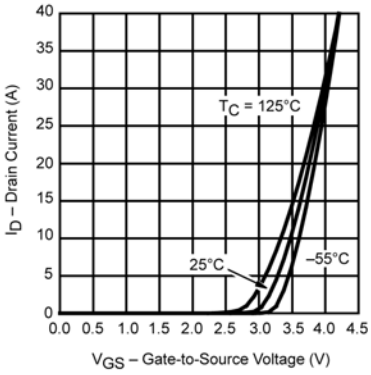
Notes

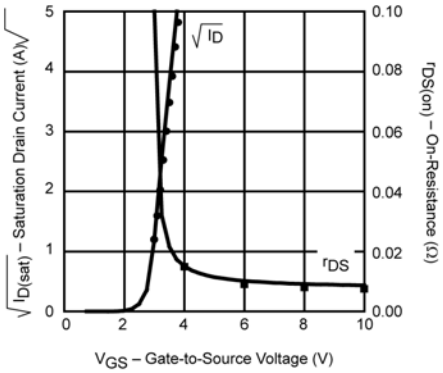
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

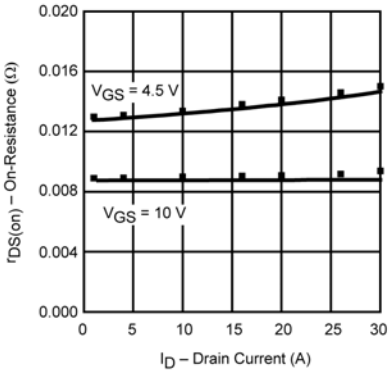
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

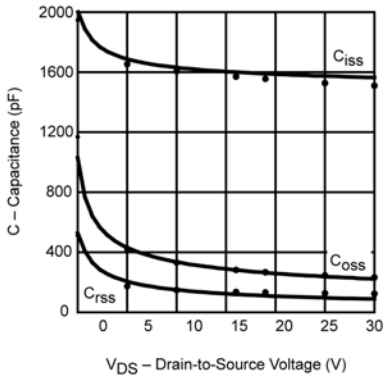
Channel 1

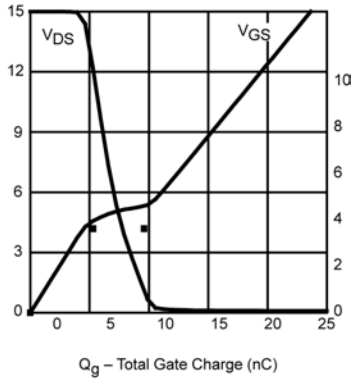






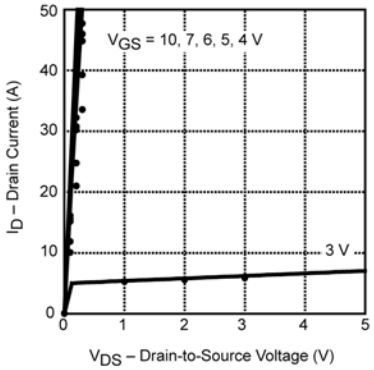


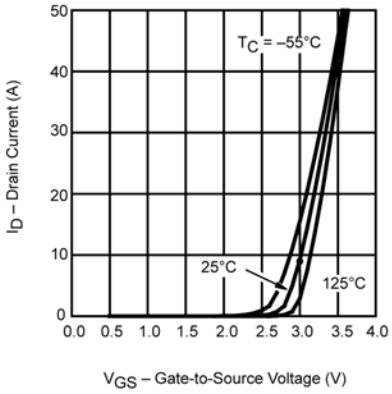


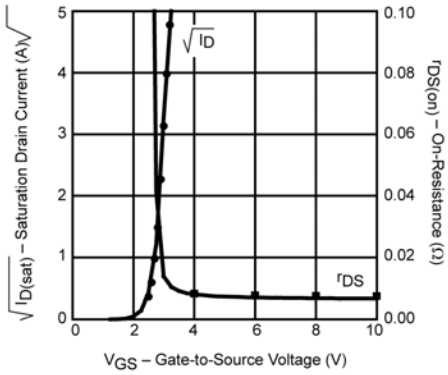


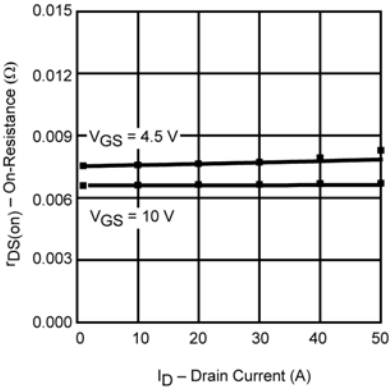
Note: Dots and squares represent measured data.

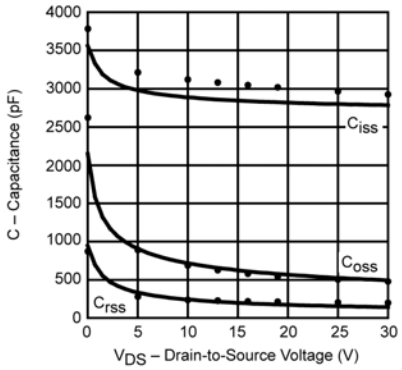
Channel 2

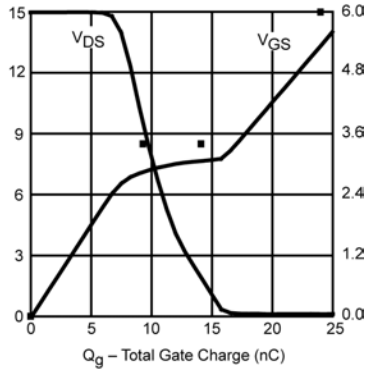












Note: Dots and squares represent measured data.

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