RoHS

HALOGEN

FREE



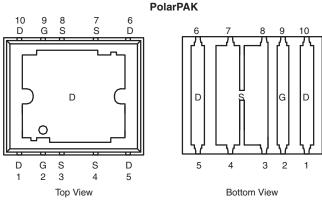


N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY					
		I _D (A) ^a			
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	Silicon Limit	Package Limit	Q _g (Typ.)	
30	0.0072 at $V_{GS} = 10 \text{ V}$	90	50	12 nC	
30	0.0115 at $V_{GS} = 4.5 \text{ V}$	73	50	12110	

Package Drawing

www.vishay.com/doc?73398



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE800DF-T1-E3 (Lead (Pb)-free)

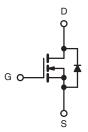
SiE800DF-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q_{gd} for Low Switching Losses TrenchFET® Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK® Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package
 - Die Not Exposed
 - Same Layout Regardless of Die Size
- Low Q_{qd}/Q_{qs} Ratio Helps Prevent Shoot-Through
- 100 % R_a and UIS Tested
- Compliant to RoHS Directive 2002/95/EC

APPLICATIONS

- **VRM**
- DC/DC Conversion: High-Side
- Synchronous Rectification



N-Channel MOSFET For Related Documents www.vishay.com/ppg?74414

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	30	V		
Gate-Source Voltage		V _{GS}	± 20	v		
	T _C = 25 °C		90 (Silicon Limit)			
	10 = 25 0		50 ^a (Package Limit)			
Continuous Drain Current (T _J = 150 °C)	T _C = 70 °C	I _D	50 ^a			
	T _A = 25 °C		20.6 ^{b, c}			
	T _A = 70 °C		16.5 ^{b, c}	Α		
Pulsed Drain Current		I _{DM}	60			
Continuous Source-Drain Diode Current	T _C = 25 °C		50 ^a			
	T _A = 25 °C	I _S	4.3 ^{b, c}			
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	40			
Avalanche Energy L = 0.		E _{AS}	80	mJ		
	T _C = 25 °C		104			
Maximum Dawar Dissination	T _C = 70 °C	P _D	66	w		
Maximum Power Dissipation	T _A = 25 °C	D	5.2 ^{b, c}	VV		
	T _A = 70 °C	1	3.3 ^{b, c}			
Operating Junction and Storage Temperature Range		T _J , T _{stg}	T _J , T _{sta} - 55 to 150			
Soldering Recommendations (Peak Temperature) ^{d, e}			260	°C		

Notes:

- a. Package limited is 50 A.
- b. Surface mounted on 1" x 1" FR4 board.
- d. See solder profile (www.vishay.com/doc?73257). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SiE800DF

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THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b} $t \le 10 \text{ s}$		R_{thJA}	20	24	
Maximum Junction-to-Case (Drain Top) ^a		R _{thJC} (Drain)	1	1.2	°C/W
Maximum Junction-to-Case (Source) ^{a, c}	Steady State	R _{thJC} (Source)	2.8	3.4	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. Maximum under steady state conditions is 68 °C/W.
- c. Measured at source pin (on the side of the package).

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static				•			
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	J 050 ·· A		34.5		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250 \mu A$		- 6.7			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu A$	1.5	2.2	3.0	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			1 10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	25		-	Α	
_	` ′	V _{GS} = 10 V, I _D = 11 A		0.006	0.0072	72 Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 9 \text{ A}$		0.0095	0.0115		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 11 A		50		S	
Dynamic ^b	9.0	50 5	l				
Input Capacitance	C _{iss}			1600			
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		750		pF	
Reverse Transfer Capacitance	C _{rss}			120			
Total Gate Charge	Qg	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 18.5 A		23	35	nC	
				12	18		
Gate-Source Charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 18.5 \text{ A}$		5.6	_		
Gate-Drain Charge	Q _{gd}			3			
Gate Resistance	R _q	f = 1 MHz		1.3	1.95	Ω	
Turn-On Delay Time	t _{d(on)}			20	30		
Rise Time	ì,	V_{DD} = 15 V, R_L = 1.5 Ω		15	25		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_q = 1 \Omega$		15	25		
Fall Time	t _f	,		8	15		
Turn-On Delay Time	t _{d(on)}			15	25	ns	
Rise Time	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 1.5 \Omega$		15	25		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		25	40		
Fall Time	t _f	-		10	15		
Drain-Source Body Diode Characteristic	cs			•			
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			50	۸	
Pulse Diode Forward Current ^a	I _{SM}				60	Α	
Body Diode Voltage	V_{SD}	I _S = 10 A		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			45	70	ns	
Body Diode Reverse Recovery Charge Q _{rr}		L = 10 A dl/dt = 100 A/up T = 05 °C		41	65	nC	
Reverse Recovery Fall Time	t _a	$I_F = 10 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		21		ns	
Reverse Recovery Rise Time	t _b			24			

Notes

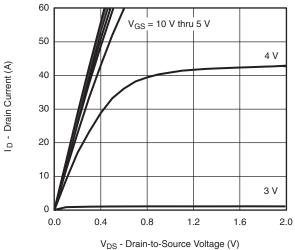
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

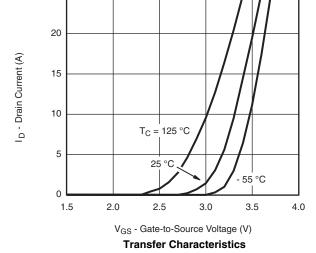




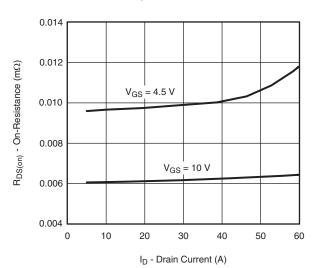
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



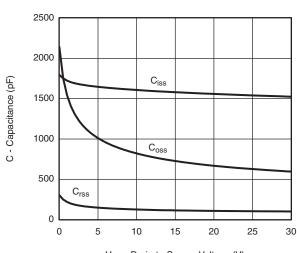
Output Characteristics



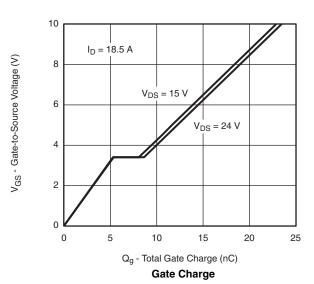
25

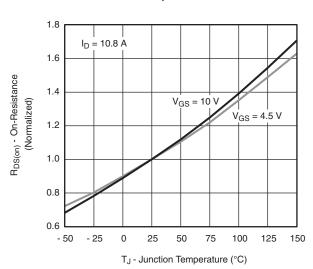


On-Resistance vs. Drain Current and Gate Voltage



 V_{DS} - Drain-to-Source Voltage (V) **Capacitance**



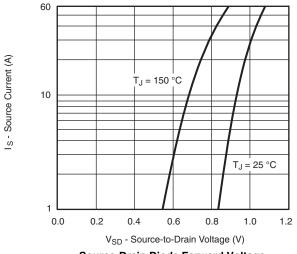


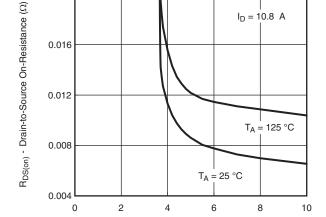
On-Resistance vs. Junction Temperature

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 $I_D = 10.8 A$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



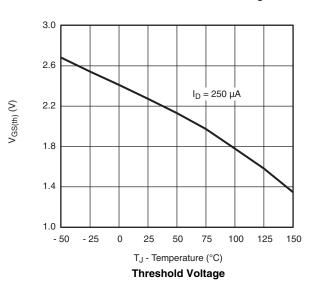


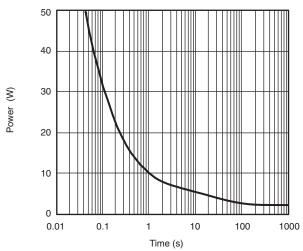
0.020

0.016

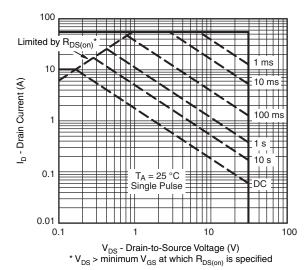
Source-Drain Diode Forward Voltage







Single Pulse Power, Junction-to-Ambient



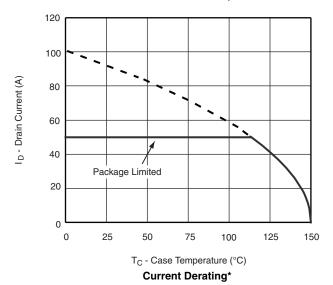
Safe Operating Area, Junction-to-Ambient

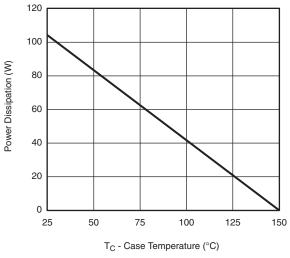






TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





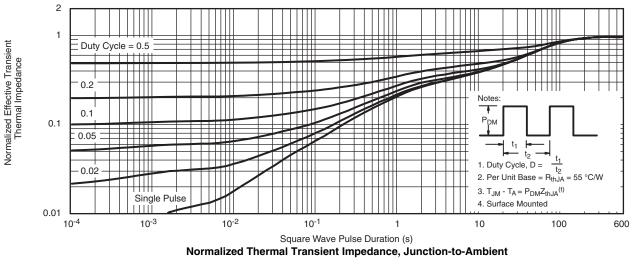
Power Derating, Junction-to-Case

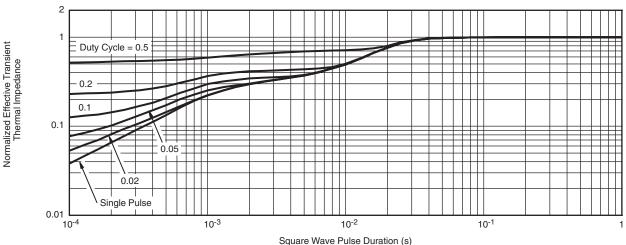
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

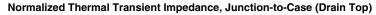
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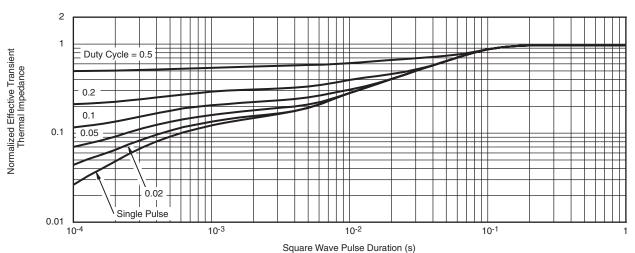
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)









Normalized Thermal Transient Impedance, Junction-to-Source

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73199.



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