Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance

By Jess Brown

INTRODUCTION

This is the second in a series of application notes that define the fundamental behavior of MOSFETs, both as standalone devices and as switching devices implemented in a Switch Mode Power Supply (SMPS). The first application note [1] provided a basic description of the MOSFET and the terminology behind the device, including definitions and physical structure. This application note goes into more detail on the switching behavior of the MOSFET when used in a practical application circuit and attempts to enable the reader/designer to choose the right device for the application using the minimum available information from the datasheet. The note goes through several methods of assessing the switching performance of the MOSFET and compares these methods against practical results. Several definitions used within the text are drawn from application note AN605.

Note

(1) AN605 Power MOSFET Basics: Understanding MOSFET Characteristics Associated with the Figure of Merit. Doc. No. 71933

SWITCHING THE MOSFET IN ISOLATION

Using Capacitance

To get a fundamental understanding of the switching behavior of a MOSFET, it is best first to consider the device in isolation and without any external influences. Under these conditions, an equivalent circuit of the MOSFET gate is illustrated in figure 1, where the gate consists of an internal gate resistance (R_g), and two input capacitors (C_{gs} and C_{gd}). With this simple equivalent circuit it is possible to obtain the output voltage response for a step gate voltage.

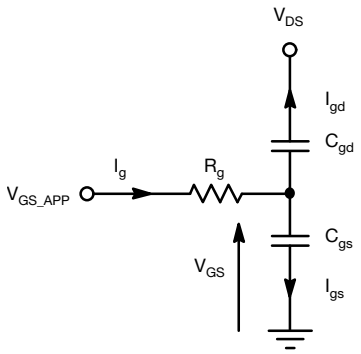


Fig. 1 - An equivalent MOSFET Gate Circuit Showing Just C_{gs}, C_{gd}, and R_g

The voltage V_{GS} is the actual voltage at the gate of the device, and it is this point that should be considered when analyzing the switching behavior of the device.

If a step input is applied at V_{GS_APP}, then the following holds true:

$$i_g = \frac{V_{GS\_APP} - V_{GS}}{R_g} \quad (1)$$

$$i_g = i_{gs} + i_{gd} \quad (2)$$

$$i_{gs} = C_{gs}\frac{dV_{GS}}{dt} \quad (3)$$

and since V_{DS} is fixed

$$i_{gs} = C_{gd}\frac{dV_{GS}}{dt} \quad (4)$$

therefore

$$\frac{V_{GS\_APP} - V_{GS}}{R_g} = C_{gs}\frac{dV_{GS}}{dt} + C_{gd}\frac{dV_{GS}}{dt} \quad (5)$$

and

$$\frac{dV_{GS}}{V_{GS\_APP} - V_{GS}} = \frac{dt}{(C_{gs} + C_{gd})R_g} \quad (6)$$

giving

$$-\ln(V_{GS\_APP} - V_{GS}) = \frac{t}{(C_{gs} + C_{gd})R_g} + k \quad (7)$$

$$V_{GS} = V_{GS\_APP} - ke^{-t/(C_{gs} + C_{gd})R_g} \quad (8)$$

at t = 0, V_{GS} = 0 V, therefore

$$V_{GS} = V_{GS\_APP}(1 - e^{-t/(C_{gs} + C_{gd})R_g}) \quad (9)$$

APPLICATION NOTE

Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance

This gives an indication of how long the actual gate voltage (V_{GS}) takes to get to the threshold voltage. For illustration purposes, a more practical circuit is shown in figure 2, where an additional resistance is placed between V_{DS} and C_{gd}. In this instance, the step response gets very complicated and the equation (equation 10) becomes very difficult to solve.

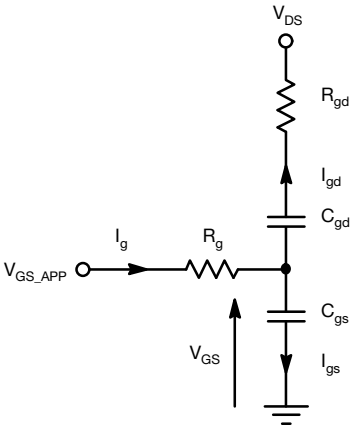


Fig. 2 - An Equivalent MOSFET Circuit Showing Just C_{gs}, C_{gd} and R_g, plus R_{gd}

$$V_{GS} = V_{GS\_APP} - \frac{V_{GS\_APP}}{2\sqrt{k}}(A - B) \qquad (10)$$

where

$$A = \left((CR_k + \sqrt{k})e - \frac{t(CR - \sqrt{k})}{2C_{gd}R_{gd}C_{gs}R_g}\right)$$

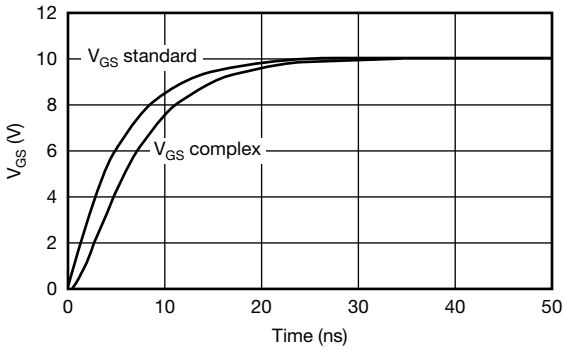
$$B = \left((CR_k - \sqrt{k})e - \frac{t(CR + \sqrt{k})}{2C_{gd}R_{gd}C_{gs}R_g}\right)$$

$$CR_k = C_{gs}R_g + C_{gd}R_g + C_{gd}R_{gd}$$

and

$$k = C_{gs}^2R_g^2 + 2C_{gs}R_g^2C_{gd} - 2C_{gd}R_{gd}C_{gs}R_g$$

$$+ C_{gd}^2R_g^2 + 2C_{gd}^2R_gR_{gd} + C_{gd}^2R_{gd}^2$$



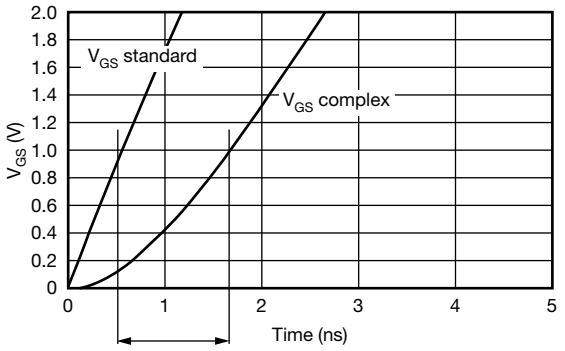


Fig. 3 - Graphs of Plots of Equations 9 (Standard) and 10 (Complex)

Plotting equations 9 and 10 in figure 3 shows that there is only about a 1ns difference in the time the gate voltage takes to get to the threshold voltage of 1 V. Therefore it can be argued that to adopt the less complex approach does not impinge significantly on the accuracy of the gate voltage transient. However, the point has been made that any calculated switching times will be less than the actual transients seen by the MOSFET.

As shown above, when the MOSFET is considered with additional parasitics, it becomes increasingly difficult to manipulate these equations manually for such a practical circuit. Therefore a method of analyzing a practical circuit is required. If these second order, or parasitic, components are ignored, then it is possible to come up with formulas for the turn-on and turn-off time periods of the MOSFET. These are given in equations 11 through to 16 and the resulting waveforms are shown in figures 4 and 5. These equations are based on those developed by B. J. Baliga [1], where R_g is the internal gate resistance, R_{g_app} is the external gate resistance, V_{th} is the MOSFET threshold voltage, and V_{GP} is the gate plateau voltage.

Note

[1] B. J. Baliga, Power Semiconductor Devices

APPLICATION NOTE

Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance

$$t_1 = (R_g + R_{g\_app})(C_{gs} + C_{gd})\ln\left(\frac{1}{1 - \frac{V_{th}}{V_{GS\_APP}}}\right) \quad (11)$$

$$t_2 = (R_g + R_{g\_app})(C_{gs} + C_{gd})\ln\left(\frac{1}{1 - \frac{V_{GP}}{V_{GS\_APP}}}\right) \quad (12)$$

$$t_3 = \frac{(V_{DS} - V_F)(R_g + R_{g\_app})C_{gd}}{V_{GS\_APP} - V_{GP}} \quad (13)$$

V_F is the voltage across the MOSFET when conducting full load current and V_{DS} is the voltage across the MOSFET when it is off.

This gives an accurate t_1 and t_2 when using datasheet values, but the time period t_3 is difficult to calculate since C_{gd} changes with V_{DS}.

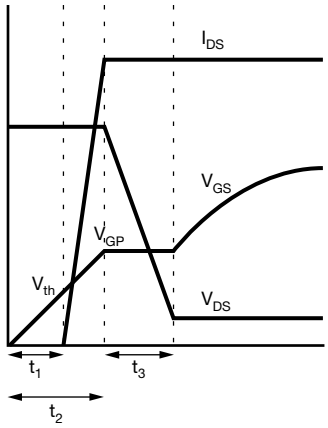


Fig. 4 - Turn-On Transient of the MOSFET

Using the same principles for turn-off, the formulas for the switching transients are given below:

$$t_4 = (R_g + R_{g\_app})(C_{gd} + C_{gs})\ln\left(\frac{V_{GS\_APP}}{V_{GP}}\right) \quad (14)$$

$$t_4 = (R_g + R_{g\_app})C_{gd}\left(\frac{V_{DS} - V_F}{V_{GP}}\right) \quad (15)$$

$$t_6 = (R_g + R_{g\_app})(C_{gd} + C_{gs})\left(\frac{V_{GP}}{V_{th}}\right) \quad (16)$$

In this instance, t_4 and t_6 can be calculated accurately, but it is the formula for t_5 which is more difficult to solve, since during this time period V_{DS} will change, causing C_{gs} to also change. Therefore some method is required to calculate t_3 and t_5 without using the dynamic C_{gd}.

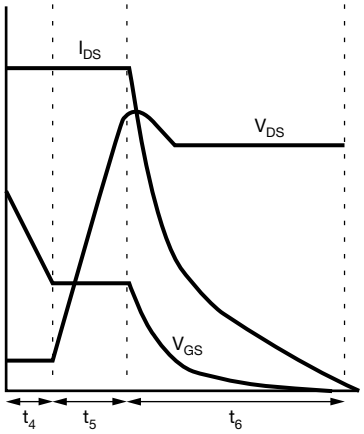


Fig. 5 - Turn-Off Transient of the MOSFET

Using Gate Charge to Determine Switching Time

Looking at the gate charge waveform [1] in figure 6, Q_{gs} is defined as the charge from the origin to the start of the Miller Plateau (V_{GP}); Q_{gd} is defined as the charge from V_{GP} to the end of the plateau; and Q_g is defined as the charge from the origin to the point on the curve at which the driving voltage V_{GS} equals the actual gate voltage of the device.

Note

(1) Gate Charge Principles and Usage, Power Electronics Europe. Issue 3, 2002. Technology.

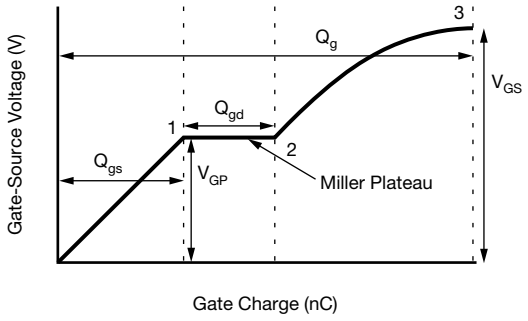


Fig. 6 - Sketch Showing Breakdown of Gate Charge

APPLICATION NOTE

Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance

The rise in V_{GS} during t_2 (figure 4) is brought about by charging C_{gs} and C_{gd}. During this time V_{DS} does not change and as such C_{gd} and C_{ds} stay relatively constant, since they vary as a function of V_{DS}. At this time C_{gs} is generally larger than C_{gd} and therefore the majority of drive current flows into C_{gs} rather than into C_{gd}. This current, through C_{gd} and C_{ds}, depends on the time derivative of the product of the capacitance and its voltage. The gate charge can therefore be assumed to be Q_{gs}.

The next part of the waveform is the Miller Plateau. It is generally accepted that the point at which the gate charge figure goes into the plateau region coincides with the peak value of the peak current. However, the knee in the gate charge actually depends on the product [1] ($C_{gd}V_{GD}$) with respect to time. This means if there is a small value of drain current and large value of output impedance, then I_{DS} can actually reach its maximum value after the left knee occurs. However, it can be assumed that the maximum value of the current will be close to this knee point and throughout this application note it is assumed that the gate voltage at the knee point corresponds to the load current, I_{DS}.

The slope of the Miller Plateau is generally shown to have a zero, or a near-zero slope, but this gradient depends on the division of drive current between C_{gd} and C_{gs}. If the slope is non-zero then some of the drive current is flowing into C_{gs}. If the slope is zero then all the drive current is flowing into C_{gd}. This happens if the $C_{gd}V_{GD}$ product increases very quickly and all the drive current is being used to accommodate the change in voltage across C_{gd}. As such, Q_{gd} is the charge injected into the gate during the time the device is in the Miller Plateau.

It should be noted that once the plateau is finished (when V_{DS} reaches its on-state value), C_{gd} becomes constant again and the bulk of the current flows into C_{gs} again. The gradient is not as steep as it was in the first period (t_2), because C_{gd} is much larger and closer in magnitude to that of C_{gs}.

Note

[1] Ibid.

Combination of Gate Charge and Capacitance to Obtain Switching Times

The objective of this note is to use datasheet values to predict the switching times of the MOSFET and hence allow the estimation of switching losses. Since it is the time from the end of t_1 to the end of t_3 that causes the turn-on loss, it is necessary to obtain this time (figure 4). Combining 11 and 12 it is possible to obtain the rise time of the current ($t_{ir} = t_2 - t_1$) and because V_{DS} stays constant during this time then it is possible to use the specified datasheet value of C_{iss} at the appropriate V_{DS} value. Assuming the transfer characteristic is constant, then V_{GP} can be substituted for $V_{th} + I_{DS}/g_{fs}$, hence

$$t_{ir} = (R_g + R_{g\_app})(C_{iss}{}^{\text{at } V_{DS}}) \times \ln\left(\frac{g_{fs}(V_{GS\_APP} - V_{th})}{g_{fs}(V_{GS\_APP} - V_{th}) - I_{DS}}\right) \quad (17)$$

It is difficult to use a value of C_{gd} for the fall time period of V_{DS} ($t_{vf} = t_3$). Therefore if the datasheet value of gate charge is used (Q_{gd_d}) and divided by the voltage swing seen on the drain connection (V_{DS_D} minus V_{F_D}) then this effectively gives a value for C_{gd} based on the datasheet transient.

$$t_{vf} = \frac{Q_{gd\_d}(V_{DS} - V_F)(R_g + R_{g\_app})}{(V_{DS\_D} - V_{F\_D})\left(V_{GS\_APP} - \left(V_{th} + \frac{I_{DS}}{g_{fs}}\right)\right)} \quad (18)$$

Similarly for the turn-off transition, the voltage rise time ($t_{vr} = t_5$) is:

$$t_{vr} = \frac{Q_{gd\_d}(V_{DS} - V_F)(R_g + R_{g\_app})}{(V_{DS\_D} - V_{F\_D})\left(V_{th} + \frac{I_{DS}}{g_{fs}}\right)} \quad (19)$$

and the current fall time ($t_{if} = t_6$) is:

$$t_{if} = (R_g + R_{g\_app})(C_{iss}{}^{\text{at } V_{DS}})\ln\left(\frac{\left(V_{th} + \frac{I_{DS}}{g_{fs}}\right)}{V_{th}}\right) \quad (20)$$

Comparing Equations with Datasheet Values

The definition of the turn-on and turn-off times given in the datasheet can be seen in Figure 7. These definitions can be equated to the equations described above and are shown here:

$$t_{d(on)} \approx t_1 + t_{ir} \quad (21)$$

$$t_r \approx t_{vf} \quad (22)$$

$$t_{d(off)} \approx t_4 \quad (23)$$

$$t_f \approx t_{vr} \quad (24)$$

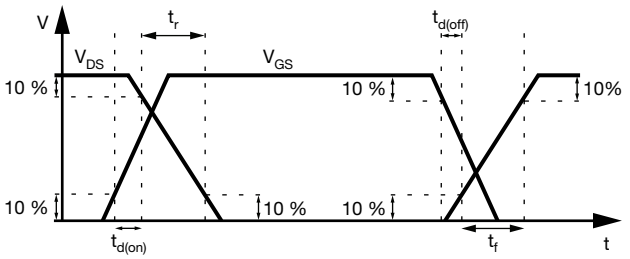


Fig. 7 - Sketch Showing Definition of Turn-On and Turn-Off Times

APPLICATION NOTE

Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance

TABLE 1 - WORKED EXAMPLE FOR SWITCHING TRANSIENTS: Si4892DY				
CALCULATIONS	**MIN.**	**TYP.**	**MAX.**	**UNIT**
R_g	0.6	0.8	1	Ω
R_{g_app}	5.4	6	6.6	
C_{iss} at V_{DS}	620	775	930	pF
C_{iss} at 0 V	880	1100	1320	
g_{fs}	21.6	27	32.4	S
V_{GS_APP}	9	10	11	V
V_{th}	0.8	1.4	1.8	
I_{DS}	0.9	1	1.1	A
Q_{gd_d}	2.8	3.5	4.2	nC
V_{DS_D}	13.5	15	16.5	V
I_{DS_D}	11.2	12.4	13.6	A
$R_{DS(on)}$	0.008	0.01	0.012	Ω
V_F	0.0072	0.01	0.0132	V
V_{F_D}	0.09	0.12	0.16	
V_{DS}	13.5	15	16.5	
t_1 (equation 11)	0.28	0.79	1.6	ns
t_{ir} (equation 17)	0.01	0.02	0.05	
t_{vf} (equation 18)	1.4	2.8	5.5	
t_4 (equation 14)	8.4	14.5	26	
t_{vr} (equation 19)	7.5	16.7	47.7	
t_{if} (equation 20)	0.06	0.14	0.44	
$t_{d(on)}$	0.29	0.81	1.7	
t_r	1.4	2.8	5.5	
$t_{d(off)}$	8.4	14.5	26	
t_f	7.5	16.7	47.7	
DATASHEET				
$t_{d(on)}$	-	10	20	ns
t_r	-	11	20	
$t_{d(off)}$	-	24	50	
t_f	-	10	20	

The minimum switching transients were calculated using the appropriate value of the parameters, which resulted in producing the shortest switching transient value. In some circumstances this meant that the maximum value of a parameter was used to calculate the minimum switching transient and vice versa for the maximum switching transients.

Comparing Equations with Measured Switching Transients

The datasheet switching transients are measured with a resistive load and are not truly representative of a practical circuit. As such the device will not behave according to the ideal operation described above. Therefore, actual switching waveforms were measured, and these are shown in figures 8 and 9. These switching transients are for the Si4892DY implemented on the high-side of a buck converter configuration. The circuit parameters were:

V_{DS} = 5 V, I_{DS} = 5 A, V_{GS_APP} = 5 V, and R_{g_app} = 10 Ω

Fig. 8 - Measured Current and Voltage Turn-On Switching Transient

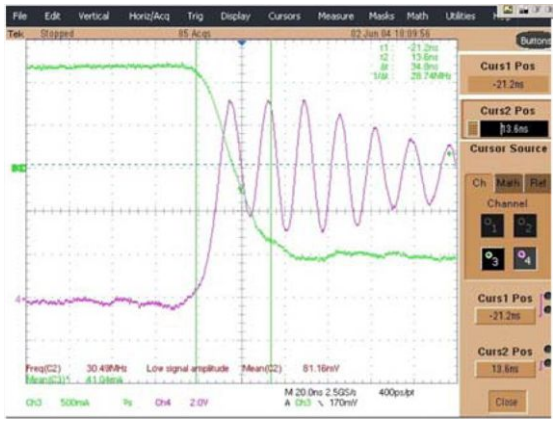


Fig. 9 - Measured Current and Voltage Turn-Off Switching Transient

TABLE 2 - MEASURED VS. CALCULATED				
CALCULATIONS	**MIN.**	**TYP.**	**MAX.**	**UNIT**
t_{ir} (equation 17)	0.18	0.44	1.1	ns
t_{vf} (equation 18)	1.6	3.7	8.4	
t_{vr} (equation 19)	3.5	7.9	22	
t_{if} (equation 20)	0.95	1.0	1.5	
MEASURED				
t_{ir}	16	20	24	ns
t_{vf}	8.8	11	13.2	
t_{vr}	10.4	13	15.6	
t_{if}	28	35	42	

APPLICATION NOTE

Power MOSFET Basics: Understanding Gate Charge and Using it to Assess Switching Performance

Limitations of the Driving Circuit

Table 2 shows the comparison between the calculations and the measured transients. It can be seen that the voltage transients are relatively close. However, the switching times of the MOSFET are affected not only by the parasitic elements, but also by the driving circuit. Under the conditions described above, the author has assumed that the gate circuit does not limit the switching performance of the power MOSFET. For example, with a MOSFET p-channel and n-channel driver, it is possible that the theoretical current into the gate will be larger than that which the driver is able to supply. There are several ways in which a MOSFET driver can be realized and this goes beyond the study of this application note. The formulas described in the text are used to gauge the switching times and therefore estimate the switching losses without navigating complex formulas, models and expensive simulation software.

The major discrepancy is between the calculated and actual current transients. These calculations are an order of magnitude less than the actual transients. Therefore, further consideration has to be taken for the current rise and fall times and this is described below.

Current Transients

The discrepancy between the calculated and the measured occurs because the calculations assume an ideal situation. One major parameter that can be considered into the equations is the package inductance of the MOSFET. This will slow the current transient and can be taken into account with relative ease if a few assumptions are made.

Since the load current will generally be much larger than the gate current, it is assumed that all the current through the package inductance will be I_{DS}. Therefore it can be shown that the voltage across the package inductance of the MOSFET during turn-on will be:

$$V_L = \frac{(V_{GS\_APP} - V_{th})g_{fs}L}{(R_g + R_{g\_app})C_{iss}{}^{at\ V_{DS}}} \times e^{-t}/(R_g + R_{g\_app})(C_{iss}{}^{at\ V_{DS}}) \quad (25)$$

This is the voltage that occurs from the current transient and as such subtracts from the gate voltage and hence slows down the current transient.

If equation 25 is subtracted from V_{GS} and solved for t, the t_{ir} transient is:

$$t_{ir} = (R_g + R_{g\_app})C_{iss}{}^{at\ V_{DS}} \times \ln\left(\frac{(V_{GS\_APP} - V_{th}) + \frac{(V_{GS\_APP} - V_{th})g_{fs}L}{(R_g + R_{g\_app})C_{iss}{}^{at\ V_{DS}}}}{(V_{GS\_APP} - V_{GP})}\right) \quad (26)$$

Applying the same principle for tif results in a current transient as follows:

$$t_{if} = (R_g + R_{g\_app})C_{iss}{}^{at\ V_{DS}} \times \ln\left(\frac{V_{GP}\left(1 + \frac{g_{fs}L}{(R_g + R_{g\_app})C_{iss}{}^{at\ V_{DS}}}\right)}{V_{th}}\right) \quad (27)$$

TABLE 3 - MEASURED VS. CALCULATED WITH PACKAGE INDUCTANCE

CALCULATIONS	MIN.	TYP.	MAX.	UNIT
t_{ir} (equation 26)	4.7	8.1	13.2	ns
t_{vf} (equation 18)	1.6	3.7	8.4	
t_{vr} (equation 19)	3.5	7.9	22	
t_{if} (equation 27)	8.1	17.9	32.8	
MEASURED				
t_{ir}	16	20	24	ns
t_{vf}	8.8	11	13.2	
t_{vr}	10.4	13	15.6	
t_{if}	28	35	42	

CONCLUSION

This application note shows good approximations for the rise and fall times of the power MOSFET, when evaluated in isolation. Datasheet values for the formulas derived can be used to get a reasonable indication of the switching performance of the MOSFET as well as the switching losses. However, as illustrated in figure 3, the ideal switching transients will always be shorter than those actually achieved, so the maximum parameters from the datasheet should always be used to give realistic results.

APPLICATION NOTE