



N- and P-Channel 40-V (D-S) MOSFET

CHARACTERISTICS

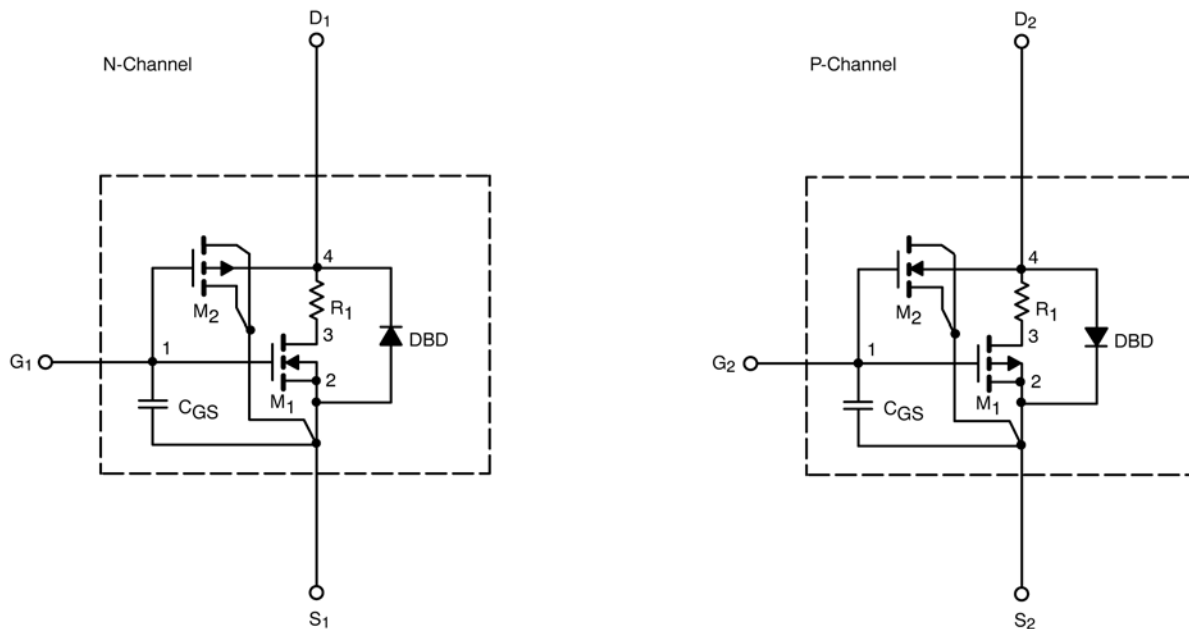
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition		Simulated Data	Measured Data	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1		V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	1.5		
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	N-Ch	63		A
		V _{DS} = -5 V, V _{GS} = -10 V	P-Ch	107		
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 5.2 A	N-Ch	0.033	0.033	Ω
		V _{GS} = -10 V, I _D = -4.5 A	P-Ch	0.044	0.045	
		V _{GS} = 4.5 V, I _D = 4.9 A	N-Ch	0.037	0.037	
		V _{GS} = -4.5 V, I _D = -3.9 A	P-Ch	0.058	0.059	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5.2 A	N-Ch	6	18	S
		V _{DS} = -15 V, I _D = -4.5 A	P-Ch	13	13	
Diode Forward Voltage ^a	V _{SD}	I _S = 1.7 A, V _{GS} = 0 V	N-Ch	0.74	0.75	V
		I _S = -1.7 A, V _{GS} = 0 V	P-Ch	0.80	-0.79	
Dynamic^b						
Input Capacitance	C _{ISS}	N-Channel V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = -20 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	863	700	pF
Output Capacitance	C _{OSS}		P-Ch	861	805	
			N-Ch	81	76	
Reverse Transfer Capacitance	C _{RSS}		P-Ch	124	120	
			N-Ch	42	45	
			P-CH	88	85	
Total Gate Charge	Q _g	N-Channel V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 5.2A P-Channel V _{DS} = -20 V, V _{GS} = -4.5 V, I _D = -4.5 A	N-Ch	7.8	8	nC
Gate-Source Charge	Q _{gs}		P-Ch	9	9	
			N-Ch	1.5	1.5	
Gate-Source Charge	Q _{gs}		P-Ch	2	2	
			N-Ch	2.4	2.4	
			P-Ch	3.6	3.6	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

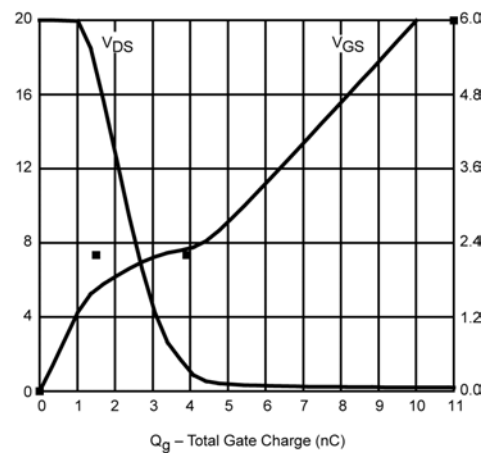
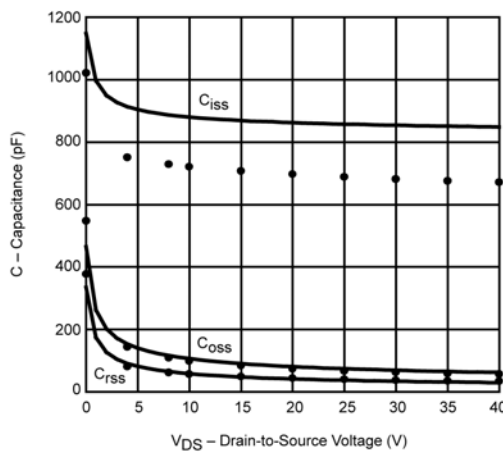
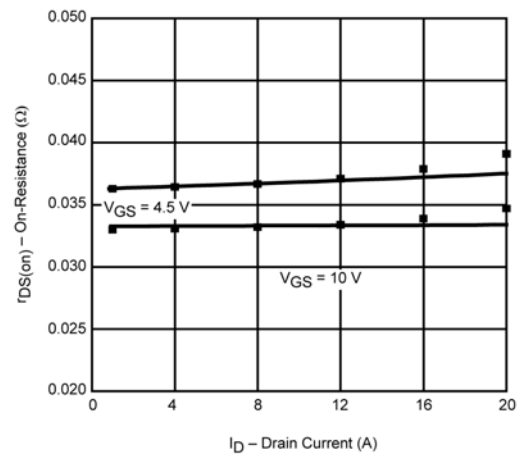
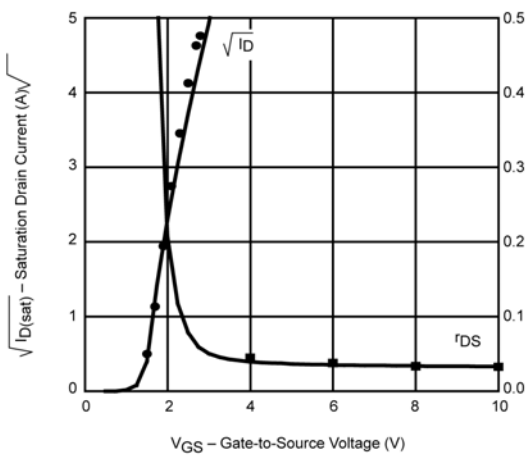
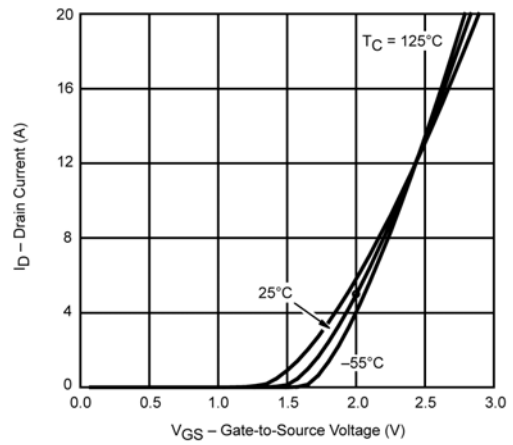
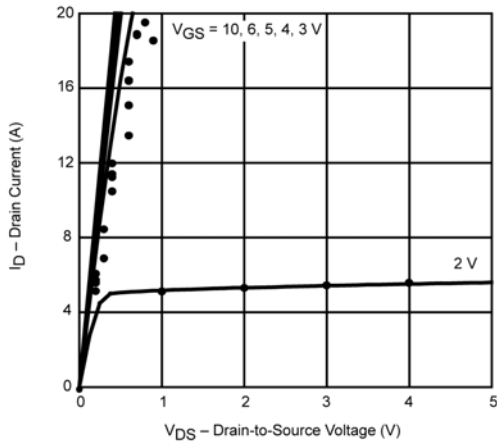


SPICE Device Model Si4565DY

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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

N-Channel MOSFET



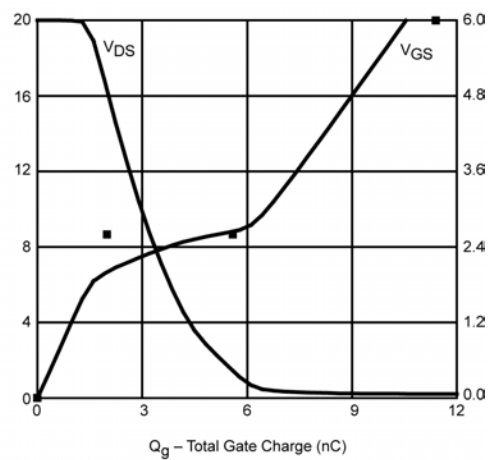
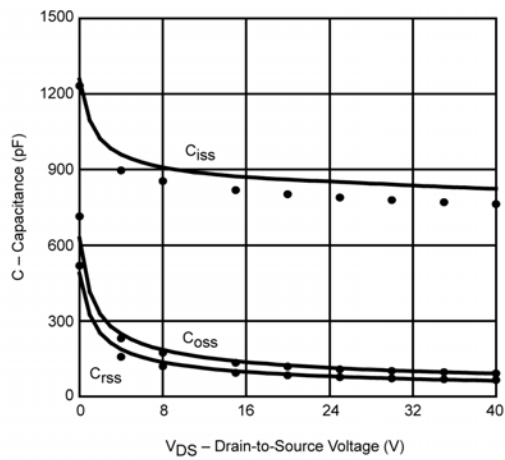
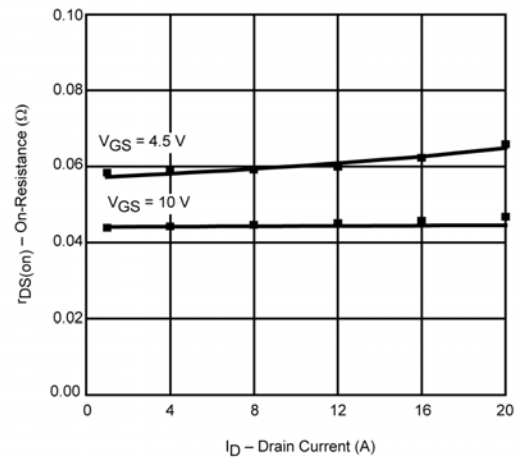
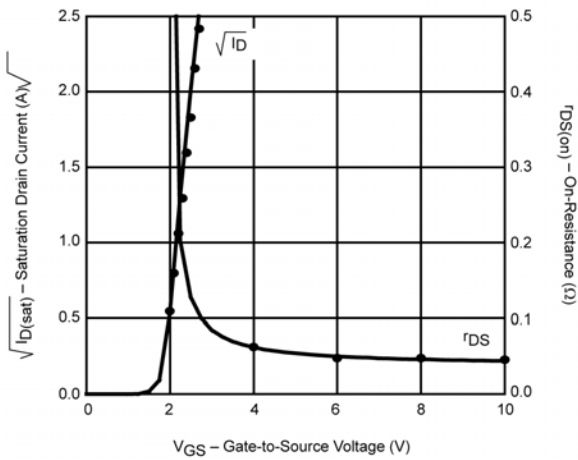
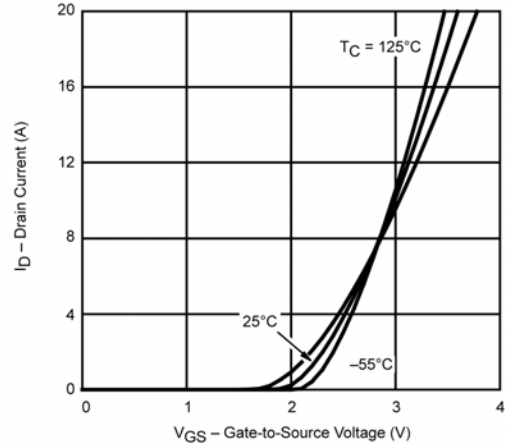
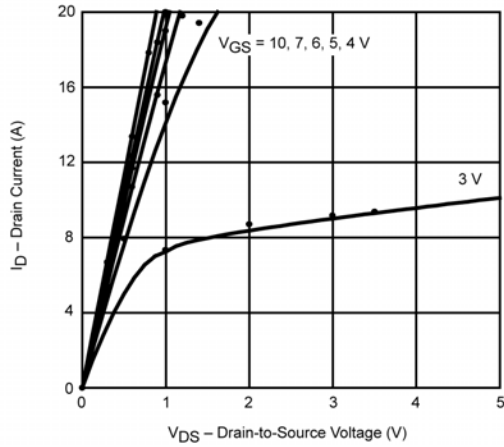
Note: Dots and squares represent measured data.

SPICE Device Model Si4565DY

Vishay Siliconix



P-Channel MOSFET



Note: Dots and squares represent measured data.



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