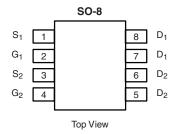




Dual N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A) ^a	Q _g (Typ.)		
60	0.058 at V _{GS} = 10 V	5.3	13 nC		
00	0.072 at V _{GS} = 4.5 V	4.7	13110		



Ordering Information: Si4900DY-T1-E3 (Lead (Pb)-free)

Si4900DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

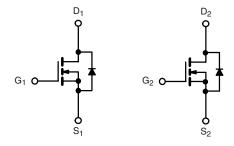
FEATURES

- Halogen-free According to IEC 61249-2-21 Available
- TrenchFET® Power MOSFET

ROHS COMPLIANT HALOGEN FREE

APPLICATIONS

• LCD TV CCFL Inverter



N-Channel MOSFET

N-Channel MOSFET

Parameter		Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage		V _{GS}	± 20	v
	T _C = 25 °C		5.3	
Continuous Drain Current /T 150 °C)	T _C = 70 °C		4.3	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	4.3 ^{b, c}	
	T _A = 70 °C		3.4 ^{b, c}	
Pulsed Drain Current (10 μs Width)	I _{DM}	20	A	
Continuous Course Ducis Diada Current	T _C = 25 °C		2.6	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	1.7 ^{b, c}	
Avalanche Current	. 04	I _{AS}	11	
Single-Pulse Avalanche Energy	L = 0 1 mH	E _{AS}	6.1	mJ
	T _C = 25 °C		3.1	
Maximum Power Dissipation	T _C = 70 °C	В	2	14/
	T _A = 25 °C	P _D	2 ^{b, c}	W
	T _A = 70 °C		1.3 ^{b, c}	
Operating Junction and Storage Temperature R	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient ^{a, d}		R _{thJA}	55	62.5	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	33	40	O/ VV	

Notes:

- a. Based on $T_C = 25$ °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s
- d. Maximum under Steady State conditions is 110 °C/W.

Si4900DY

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SPECIFICATIONS T _J = 25 °C							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	1					ı	
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	60			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I _D = 250 μA		55		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	_ ,		- 6			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1		3	V	
	* GS(III)	$V_{DS} = V_{GS}$, $I_D = 5 \text{ mA}$		2.5		, v	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$			100	nA	
Zero Gate Voltage Drain Current	l	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$			1 μA		
Zero date voltage Brain Garrent	IDSS	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 85 ^{\circ}\text{C}$			10	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 V$, $V_{GS} = 10 V$	20			Α	
Dunin Course On Chata Basistana a	В	$V_{GS} = 10 \text{ V}, I_D = 4.3 \text{ A}$		0.046	0.058	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 3.9 \text{ A}$		0.059	0.072		
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_D = 4.3 \text{ A}$		15		S	
Dynamic ^b							
Input Capacitance	C _{iss}			665		pF	
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		75			
Reverse Transfer Capacitance	C _{rss}			40			
	Q _g	$V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 4.3 \text{ A}$		13	20		
Total Gate Charge				6	9		
Gate-Source Charge		V _{DS} = 30 V, V _{GS} = 4.5 V, I _D = 4.3 A		2.3		nC	
Gate-Drain Charge	Q_{gd}			2.6			
Gate Resistance	R_g	f = 1 MHz		2		Ω	
Turn-On Delay Time	t _{d(on)}			15	25		
Rise Time	t _r	V_{DD} = 30 V, R_L = 8.8 Ω		65	100	-	
Turn-Off Delay Time		$I_D \cong 3.4 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		15	25		
Fall Time	t _f			10	15		
Turn-On Delay Time	t _{d(on)}			10	15	ns	
Rise Time	t _r	V_{DD} = 30 V, R_L = 8.8 Ω		15	25		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 3.4 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		20	30		
Fall Time	t _f			10	15		
Drain-Source Body Diode Characterist	tics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			2.6		
Pulse Diode Forward Current	I _{SM}				20	A	
Body Diode Voltage	V_{SD}	I _S = 1.7 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			30	60	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	17 A dl/dt 100 A/:- T 05 00		32	50	nC	
Reverse Recovery Fall Time	ta			25		1	
Reverse Recovery Rise Time	t _b	 		5		ns	

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$

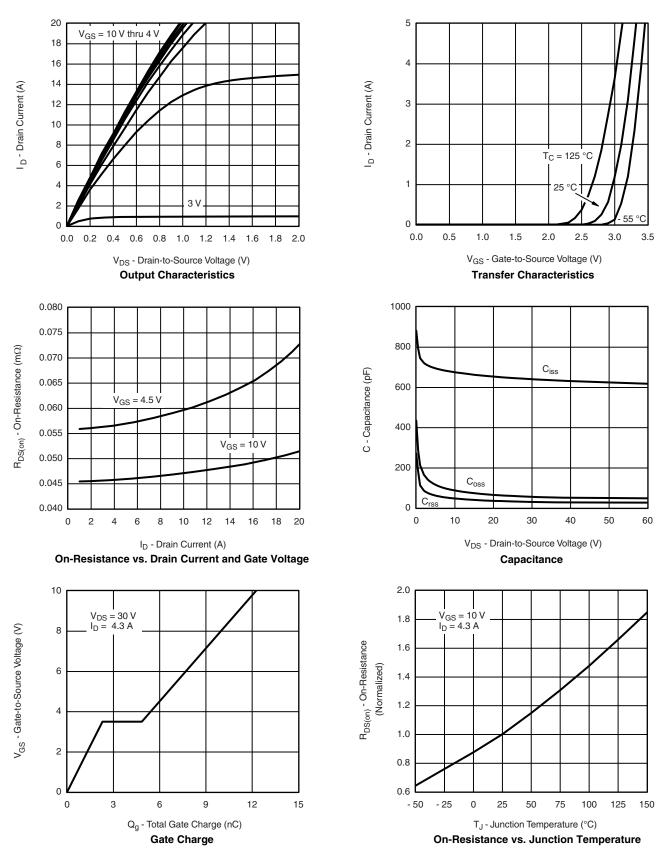
b. Guaranteed by design, not subject to production testing.





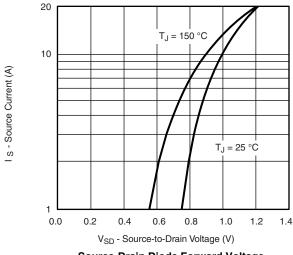


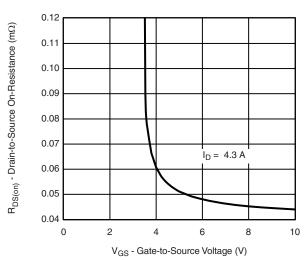
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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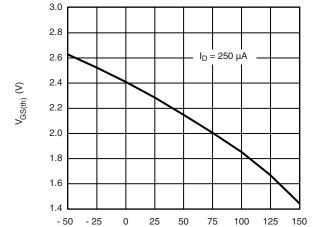
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



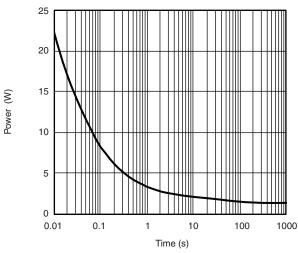


Source-Drain Diode Forward Voltage



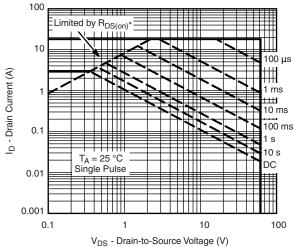


On-Resistance vs. Gate-to-Source Voltage



T_J - Temperature (°C) **Threshold Voltage**

Single Pulse Power, Junction-to-Ambient

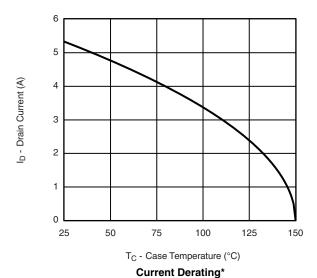


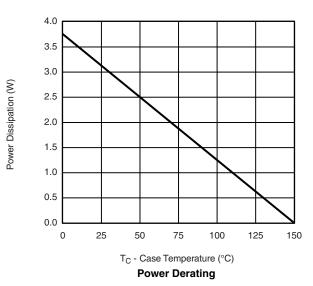
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

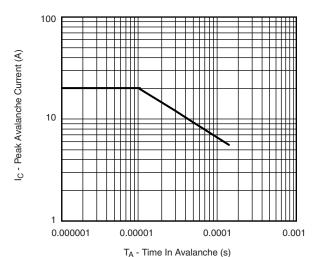
Safe Operating Area



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted







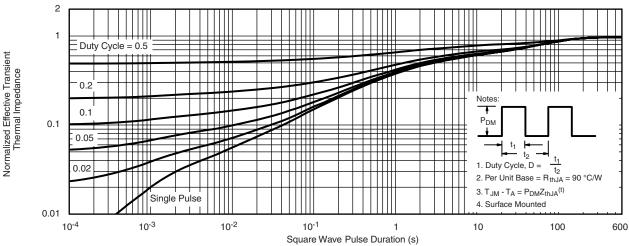
Single Pulse Avalanche Capability

^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

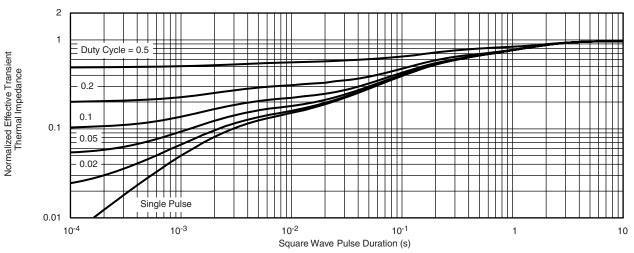
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIMETERS INCHES			HES		
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index

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