



### N- and P-Channel 60-V (D-S) MOSFET

#### CHARACTERISTICS

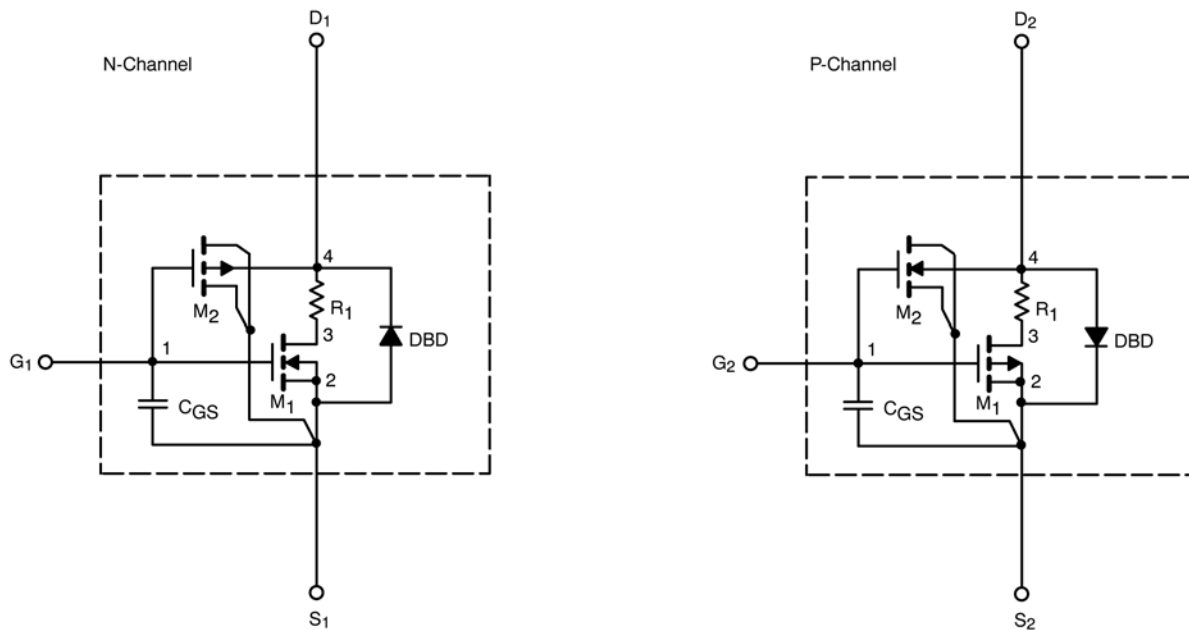
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition		Simulated Data	Measured Data	Unit
<b>Static</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	1.6		V
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	2		
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	N-Ch	80		A
		$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	P-Ch	99		
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 4.6 \text{ A}$	N-Ch	0.059	0.060	$\Omega$
		$V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$	P-Ch	0.050	0.051	
		$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$	N-Ch	0.078	0.080	
		$V_{GS} = -4.5 \text{ V}, I_D = -4.5 \text{ A}$	P-Ch	0.063	0.064	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15 \text{ V}, I_D = 4.6 \text{ A}$	N-Ch	8	6	S
		$V_{DS} = -15 \text{ V}, I_D = -5 \text{ A}$	P-Ch	15	16	
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.7 \text{ A}, V_{GS} = 0 \text{ V}$	N-Ch	0.82	0.85	V
		$I_S = -2.9 \text{ A}, V_{GS} = 0 \text{ V}$	P-Ch	0.83	-0.85	
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	$Q_g$	N-Channel $V_{DS} = 30 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$ P-Channel $V_{DS} = -30 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$	N-Ch	10	12	nC
Gate-Source Charge	$Q_{gs}$		P-Ch	24	26	
			N-Ch	2	2	
Gate-Drain Charge	$Q_{gd}$		P-Ch	4.5	4.5	
			N-Ch	3.5	3.5	
			P-Ch	7	7	

**Notes**

- a. Pulse test; pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

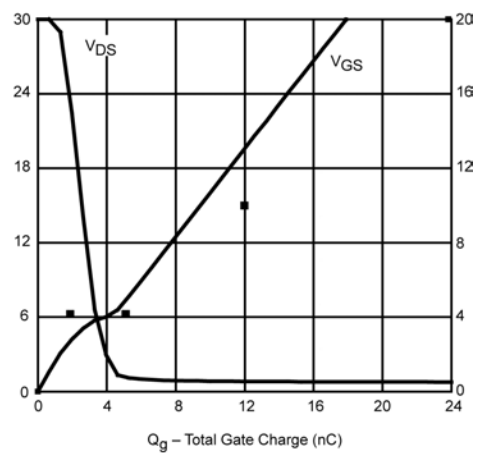
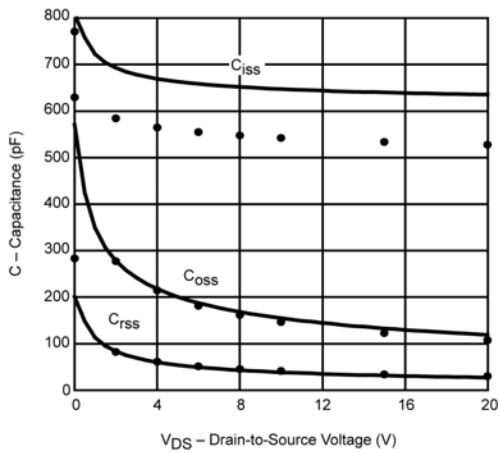
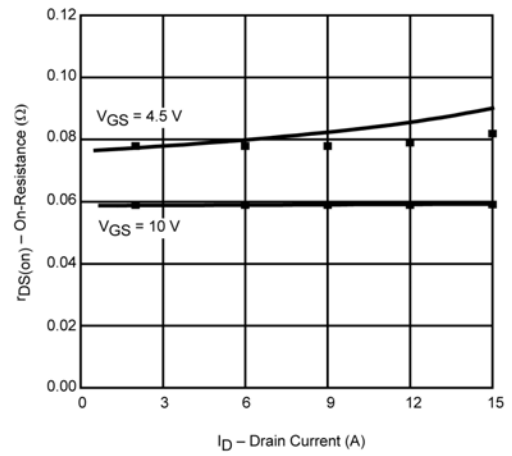
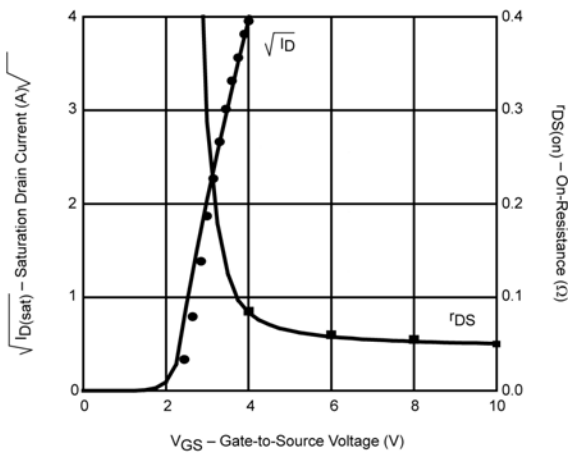
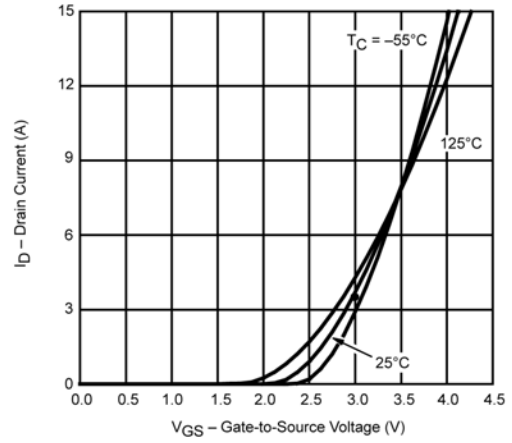
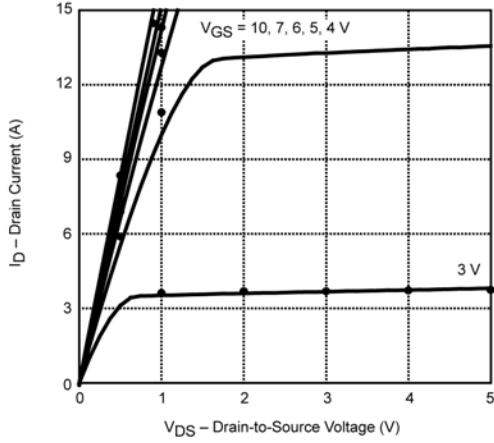


# SPICE Device Model Si7530DP

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COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

### N-Channel MOSFET



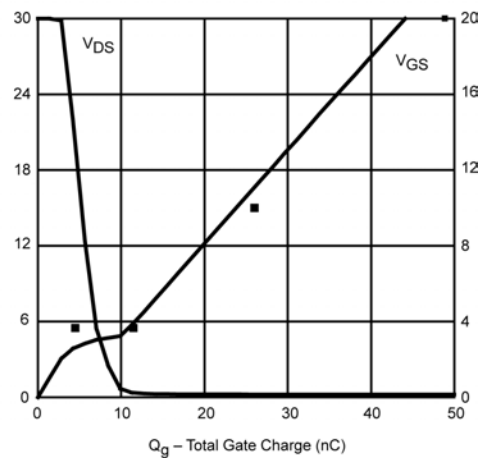
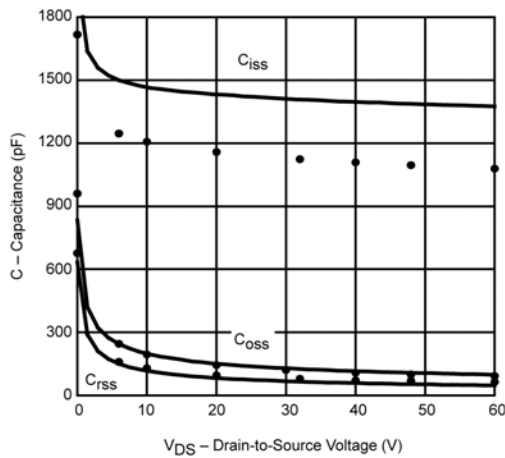
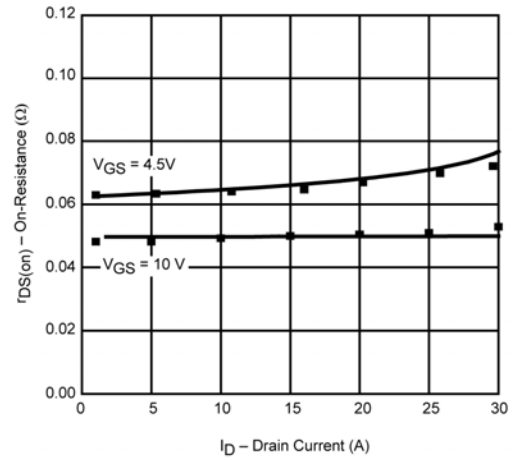
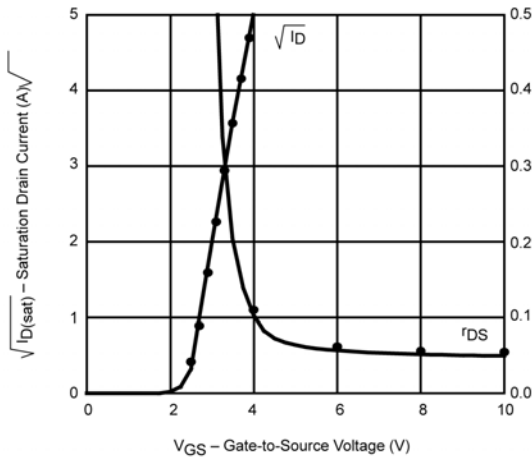
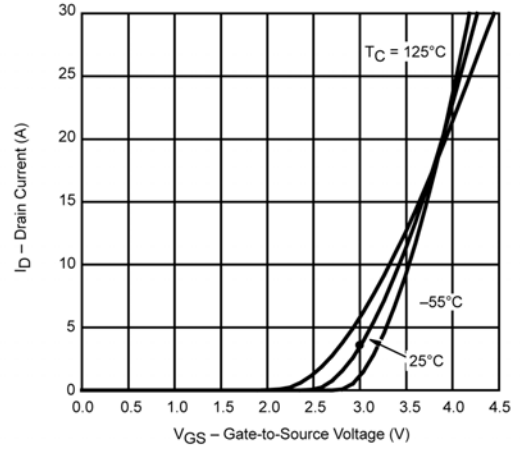
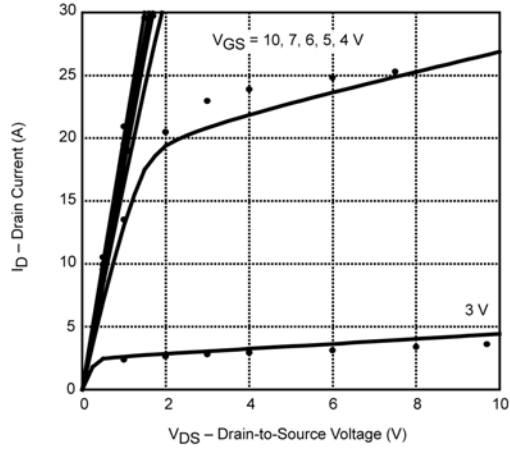
Note: Dots and squares represent measured data.

# SPICE Device Model Si7530DP

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### P-Channel MOSFET



Note: Dots and squares represent measured data.



## Disclaimer

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