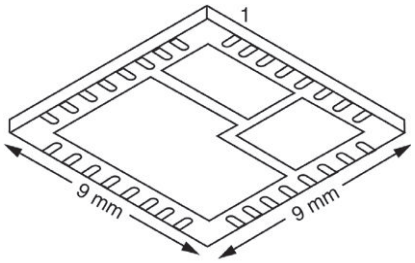
# Fast Switching MOSFETs With Integrated Driver

| PRODUCT SUMMARY | |
|---|---|
| Input Voltage Range | 3.3 to 24 V |
| Output Voltage Range | 0.5 to 6 V |
| Operating Frequency | 100 kHz to 1 MHz |
| Continuous Output Current | Up to 25 A |
| Peak Efficiency | 92.8 |
| Optimized Duty Cycle Ratio | 10 % |

**PowerPAK MLF 9 x 9**




Bottom View

**Ordering Information:** SiC734CD9-T1

## FEATURES

- Low-side MOSFET control pin for pre-bias start-up
- Undervoltage Lockout for safe operation
- Internal boostrap diode reduces component count
- Break-Before-Make operation
- Turn-on/Turn-off Capability
- Compatible with any single or multi-phase PWM controller
- Low profile, thermally enhanced PowerPAK® MLF 9 x 9 Package

## APPLICATIONS

- DC-to-DC Point-of-Load Converters
  - 3.3 V, 5 V, or 12 V Intermediate BUS
  - Examples
    - 12 $V_{IN}$/0.8 - 2.5 $V_{OUT}$
    - 5 $V_{IN}$/0.8 - 1.5 $V_{OUT}$
- Servers and Computers
- Single and Multi-Phase Conversion

## DESCRIPTION

The SiC734CD9 is an integrated solution which contains two PWM-optimized MOSFETs (high side and low side MOSFETs) and a driver IC. Integrating the driver allows better optimization of Power MOSFETs. This minimizes the losses and provides better performance at higher frequency. The SiC734CD9 is packed in Vishay Siliconix's high performance PowerPAK MLF 9 x 9 package. Compact co-packing of components helps to reduce stray inductance, and hence increases efficiency.

## FUNCTIONAL BLOCK DIAGRAM

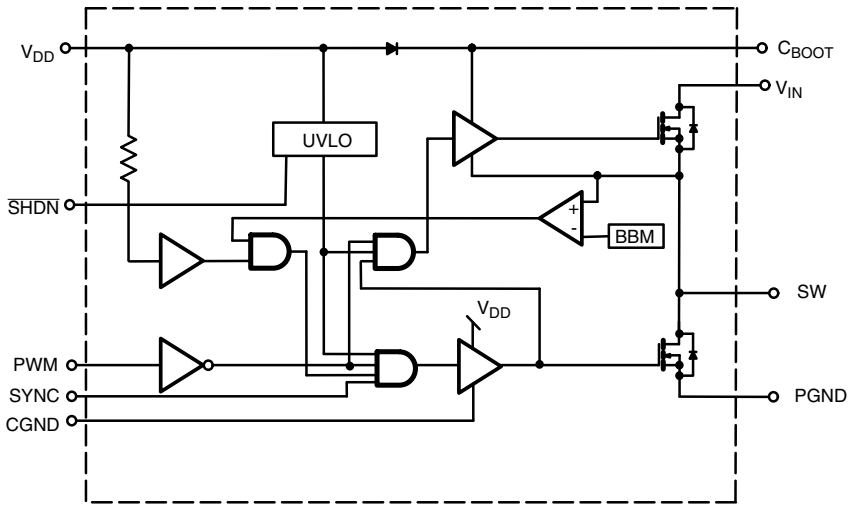



**Figure 1.**

| ABSOLUTE MAXIMUM RATINGS $T_A$ = 25 °C, unless otherwise noted | | | |
|---|---|---|---|
| **Parameter** | **Symbol** | **Steady State** | **Unit** |
| Logic Supply | $V_{DD}$ | 7 | V |
| Logic Inputs | $V_{PWM}$ | 7.3 | |
| Common Switch Node | $V_{SW}$ | 30 | |
| Drain Voltage | $V_{IN}$ | 30 | |
| Bootstrap Voltage | $C_{BOOT}$ | SW + 7 | |
| Maximum Power Sissipation (Measured at 25 °C ) | $P_D$ | 6 | W |
| Operating Juncyion and Storage Temperature Range | $T_j$, $T_{stg}$ | - 65 to 125 | °C |
| Soldering Recommendations (Peak Temperature)[a, b] | | 225 | |

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating/conditions for extended periods may affect device reliability.*

| RECOMMENDED OPERATING CONDITIONS | | | |
|---|---|---|---|
| **Parameter** | **Symbol** | **Steady State** | **Unit** |
| Drain Voltage | $V_{IN}$ | 3.3 to 24 | V |
| Logic Supply | $V_{DD}$ | 4.5 to 5.5 | |
| Input Logic PWM Voltage | $V_{PWM}$ | 5 | |
| Bootstrap Capacitor | $C_{BOOT}$ | 100 n to 1 µ | F |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **Parameter[c]** | | **Symbol** | **Typical** | **Maximum** | **Unit** |
| Maximum Junction-to-Case | Steady State | $R_{thJC}$ | 3.5 | 4.5 | °C/W |
| Maximum Junction-to-Ambient (PCB = Copper 25 mm x 25 mm) | | $R_{thJA}$ | 60 | 75 | |

Notes:

a. See Reliability Manual for profile. The PowerPAK MLF 9 x 9 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot guaranteed and is not required to ensure adequate bottom side soldering interconnection.

b. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

c. Junction-to-case thermal impedance represents the effective thermal impedance of all heat carrying leads in parallel and is intended for use in conjunction with the thermal impedance of the PC board pads to ambient ($R_{thJA}$ = $R_{thJC}$ + $R_{thPCB-A}$). It can also be used to estimate chip temperature if power dissipation and the lead temperature of heat carrying (drain) lead is known.

## SPECIFICATIONS

| Parameter | | Symbol | Test Conditions Unless Specified $T_A$ = 25 °C, 4.5 V < $V_{DD}$ < 5.5 V, 4.5 V < $V_{IN}$ < 20 V | | Limits Min | Limits Typ[a] | Limits Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **Controller** | | | | | | | | |
| Logic Voltage | | $V_{DD}$ | | | 4.5 | | 5.5 | V |
| Logic Current (Static) | | $I_{DD(EN)}$ | $V_{DD}$ = 4.5 V, SYNC = H, PWM = H, $\overline{SHDN}$ = H | | | 1185 | | µA |
| | | $I_{DD(DIS)}$ | $V_{DD}$ = 4.5 V, SYNC = H, PWM = H, $\overline{SHDN}$ = L | | | 115 | | |
| Logic Current (Dynamic) | | $I_{DD1(DYN)}$ | $V_{DD}$ = 5 V, $f_{PWM}$ = 250 kHz[c] | | | 24 | | mA |
| | | $I_{DD2(DYN)}$ | $V_{DD}$ = 5 V, $f_{PWM}$ = 700 kHz[c] | | | 52 | | |
| **Logic Input** | | | | | | | | |
| Logic Input (VPWM) | High | $V_{PWMH}$ | $V_{DD}$ = 5 V, SYNC = H, $\overline{SHDN}$ = H | | 2.5 | | | V |
| | Low | $V_{PWML}$ | | | | | 1.35 | |
| Logic Input Voltage ($V_{SYNC}$) | | $V_{SYNC}$ | $V_{DD}$ = 5 V, PMW = H, $\overline{SHDN}$ = H | | | 2.0 | | |
| Logic Input Voltage ($V_{SHDN}$) | | $V_{\overline{SHDN}}$ | $V_{DD}$ = 5 V, PMW = H, SYNC = H | | | 2.0 | | |
| Input Voltage Hysteresis (PWM) | | $V_{HYS}$ | | | | 400 | | mV |
| Logic Input Current | | $I_{\overline{SHDN}}$ | $V_{DD}$ = 5.5 V, $\overline{SHDN}$ = 0 V | | | 117 | | µA |
| | | $I_{PWM}$ | $V_{DD}$ = 5.5 V, PMW = 5.5 V | | | 114 | | |
| **Protection** | | | | | | | | |
| Break-Before-Make Reference | | $V_{BBM}$ | $V_{DD}$ = 5.5 V | | | 2.4 | | V |
| Under-Voltage Lockout | | $V_{UVLO}$ | $V_{DD}$ = 5 V, SYNC = H, $\overline{SHDN}$ = H | | 3.5 | 4.1 | 4.25 | |
| Under-Voltage Lockout Hysteresis | | $V_H$ | | | | 0.4 | | |
| **MOSFETs** | | | | | | | | |
| Drain-Source Voltage | | $V_{DS}$ | $I_D$ = 250 µA | | 30 | 32 | | V |
| Drain-Source On-State Resistance[a] | | $r_{DS(on)1}$ | $V_{DD}$ = 5 V, $I_D$ = 10 A, $T_A$ = 25 °C | High-Side | | 9.5 | 12.3 | mΩ |
| | | $r_{DS(on)2}$ | | Low-Side | | 3.7 | 4.5 | |
| Diode Forward Voltage[a] | | $V_{SD1}$ | $I_S$ = 2 A, $V_{GS}$ = 0 V | High-Side | | 0.7 | 1.1 | V |
| | | $V_{SD2}$ | | Low-Side | | 0.67 | 1.1 | |
| **Dynamic[b, c]** | | | | | | | | |
| Turn On Delay Time | | $t_{d(on)}$ | 50 % - 50 %[c] | | | 58 | | ns |
| Turn Off Delay Time | | $t_{d(off)}$ | | | | 31 | | |

Notes:
a. Pulse test; pulse width ≤ 300 ms, duty cycle ≤ 2 %.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. Using application board SiDB766706.

## TIMING DIAGRAM

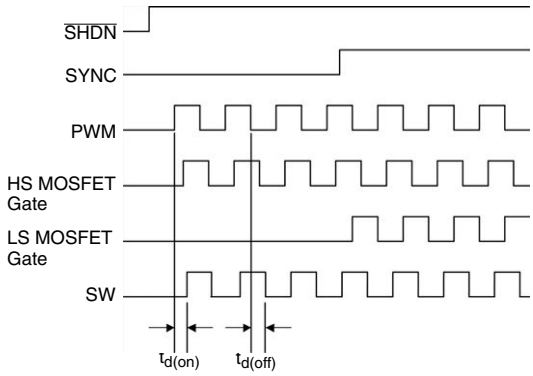



**Figure 2.**

## APPLICATION INFORMATION[a] (25 °C, unless noted, LFM = 0)

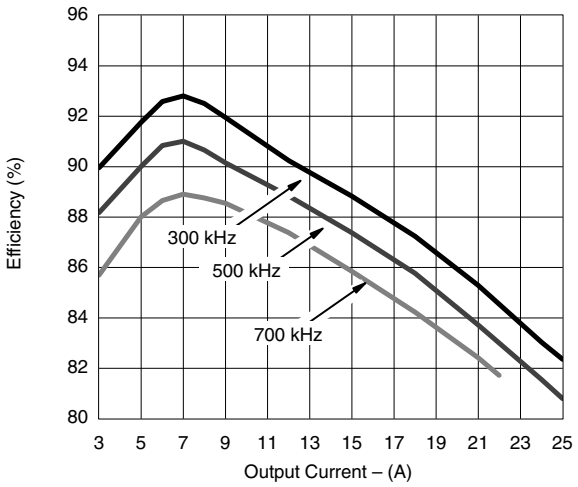



**Figure 3. Total Efficiency 12 $V_{IN}$/1.3 $V_{OUT}$**

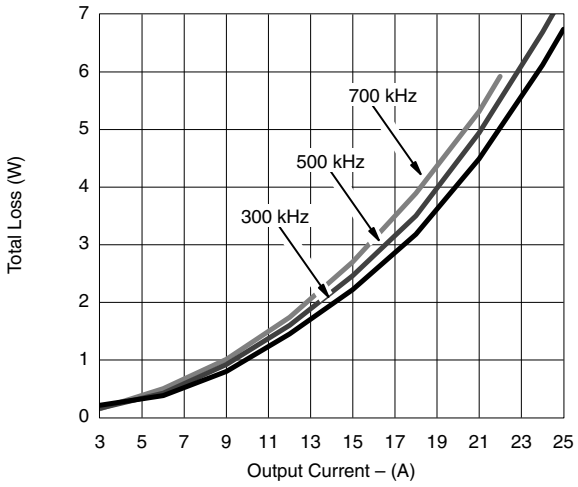


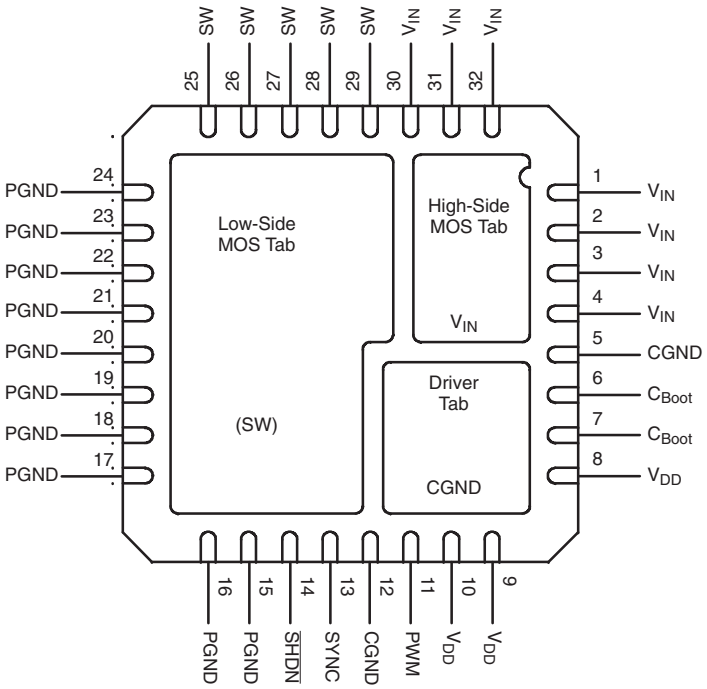

**Figure 4. Total Loss 12 $V_{IN}$/1.3 $V_{OUT}$**

Notes:

a. Experimental results using an evaluation board with a specific set of operating conditions.

## PIN CONFIGURATION

**PowerPAK MLF 9 mm x 9 mm (Bottom View)**




| TRUTH TABLE | | | | |
|---|---|---|---|---|
| $\overline{SHDN}$ | SYNC | PWM | HS MOSFET | LS MOSFET |
| L | X | X | OFF | OFF |
| H | L | L | OFF | OFF |
| H | L | H | ON | OFF |
| H | H | L | OFF | ON |
| H | H | H | ON | OFF |

| PIN DESCRIPTION | | |
|---|---|---|
| Pin Number | Symbol | Description |
| 1 - 4, 30 - 32 | $V_{IN}$ | Input-Voltage (High-Side MOSFET Drain) |
| 5, 12 | CGND | Control Ground. Should be connected to PGND externally |
| 6, 7 | $C_{BOOT}$ | Connection pin for Bootstrap Capacitor for High-Side MOSFET |
| 8, 9, 10 | $V_{DD}$ | Logic Supply Voltage - decoupling to GND with a CAP is strongly recommended |
| 11 | PMW | Pulse Width Modulation (PWM) Signal Input |
| 13 | SYNC | Disable Low-Side MOSFET Drive |
| 14 | SHDN | Disable All Functions (Active Low) |
| 15 - 24 | PGND | Power Ground (Low-Side MOSFET Source) |
| 25 - 29 | SW | Connection Pin for Output Inductor (High-Side MOSFET Source/Low-Side MOSFET Drain) |

## DEVICE OPERATION

### Pulse Width Modulator (PWM)

This is a CMOS compatible logic input that receives the drive signals from the controller circuit. The PWM signal drives the buck switch.

### Break-Before-Make (BBM)

The SiC730CD9 has an intrenal break-before-make function to ensure that both high-side and low-side MOSFETs are not turned on the same time. The low-side MOSFET will not turn on until the high-side gate drive voltage is less than $V_{BBM}$, thus ensuring that the high-side MOSFET is turned off. This parameter is not user adjustable.

### $\overline{SHDN}$

CMOS logic signal. In the low state, the $\overline{SHDN}$ disables both high-side and low-side MOSFET's.

### Capacitor to Boot Input ($C_{BOOT}$)

Connected to $V_{DD}$ by an internal diode via the $C_{BOOT}$ pin, the boot capacitor is used to sustain rail for the high-side MOSFET gate drive circuit.

### Under Voltage Lockout (UVLO)

During the start up cycle, the UVLO disables the gate drive holding high-side and low-side MOSFET's low until the input voltage rail has reached a point at which the logic circuitry can be safely activated. The UVLO is not user adjustable.

### SYNC Pin for Pre-Bias Start-Up

The low side MOSFET can be individually enable or disabled by using the SYNC pin. In the low state (SYNC = low), the low-side MOSFET is turned off. In the high state, the low-side MOSFET is enabled and follows the PWM input signal (see timing diagram, Figure 2). SYNC is a CMOS compatible logic input and is used for a pre–biased output voltage.

### Voltage Input ($V_{IN}$)

This is the power input to the drain of the high-side Power MOSFET. This pin is connected to the high power intermediate BUS rail.

### Switch Node (SW)

The Switch node is the circuit PWM regulated output. This is the output applied to the filter circuit to deliver the regulated high output for the buck converter.

### Power Ground (PGND)

This is the output connection from the source of the low-side MOSFET. This output is the ground return loop for the power rail. It should be externally connected to CGND.

### Control Ground (CGND)

This is the control voltage return path for the driver and logic input circuitry to the SiC730CD9. This should externally connected to PGND.

## APPLICATION CIRCUIT

**Power Up Sequence**: The presence of $V_{DD}$ prior to applying the $V_{IN}$ and PWM is recommended to ensure a safe turn on

**Power Down Sequence:** The sequence should be reverse of the on sequence, turn off the $V_{IN}$ before turning off the $V_{DD}$.

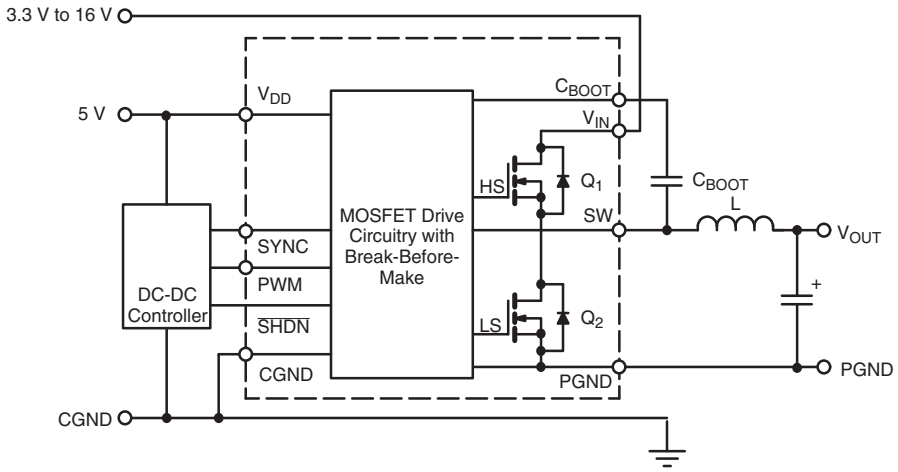



**Figure 7**

The SiC714CD10 has a built-in delay time that is optimized for the MOSFET pair. When the PWM signal goes low, the high-side driver will turn off, after circuit delay ($t_{doff}$), and the output will start to ramp down,($t_f$). After a further delay, the low-side driver turns on.

The SiC734CD9 has a built-in delay time that is optimized for the MOSFET pair. When the PWM signal goes low, the high-side driver will turn off, after circuit delay ($t_{doff}$), and the output will start to ramp down, ($t_f$). After a further delay, the low-side driver turns on.

When the PWM goes high, the low-side driver turns off,($t_{don}$). As the body diode starts to conduct, the high-side MOSFET turns on after a short delay . The delay is minimized to limit body diode conduction. The output then ramps up,($t_r$).

When the PWM goes high, the low-side driver turns off, ($t_{don}$). As the body diode starts to conduct, the high-side MOSFET turns on after a short dalay. The delay is minimized to limit body diode conduction. The output then ramps up, ($t_r$).

## TYPICAL APPLICATION

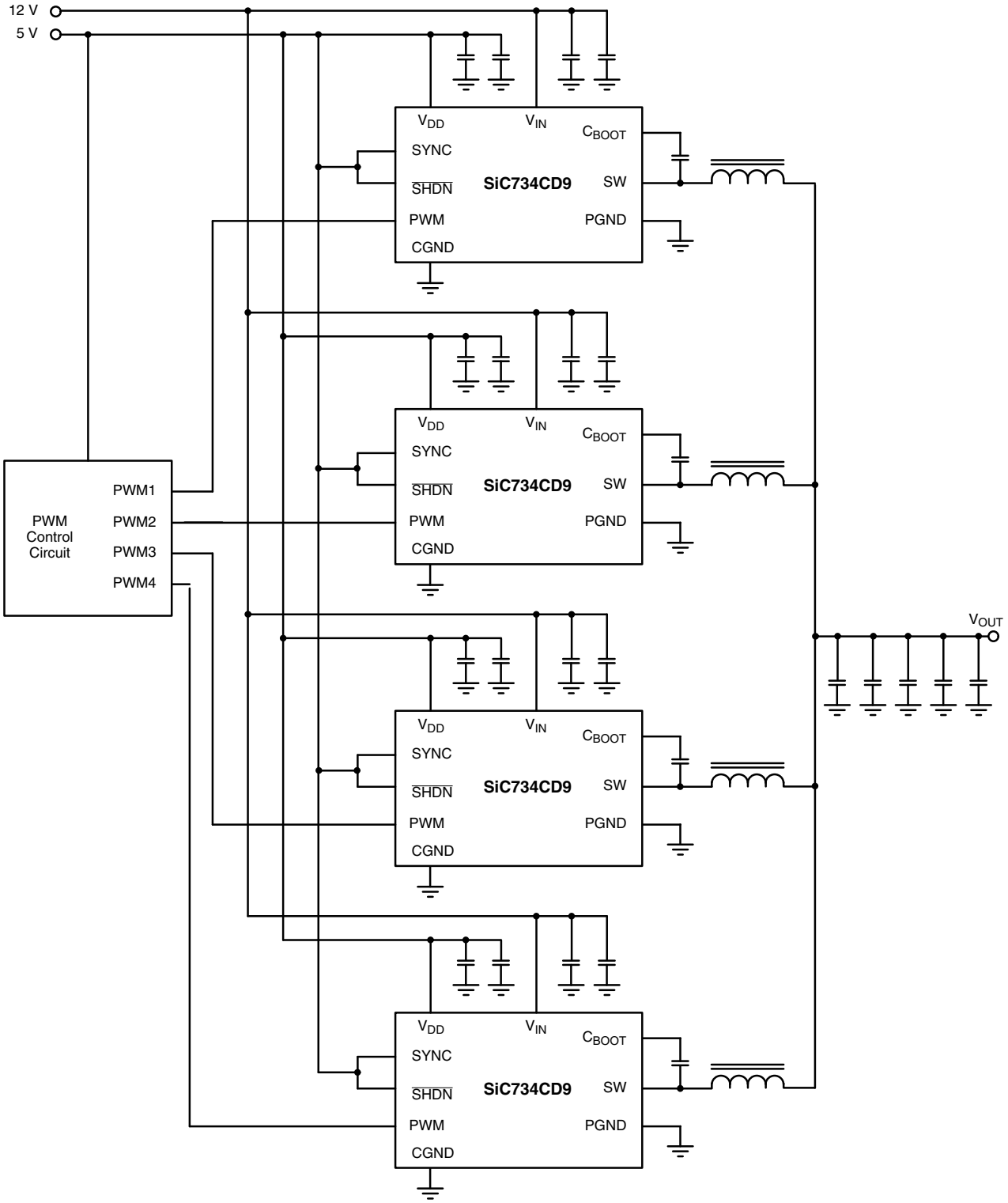
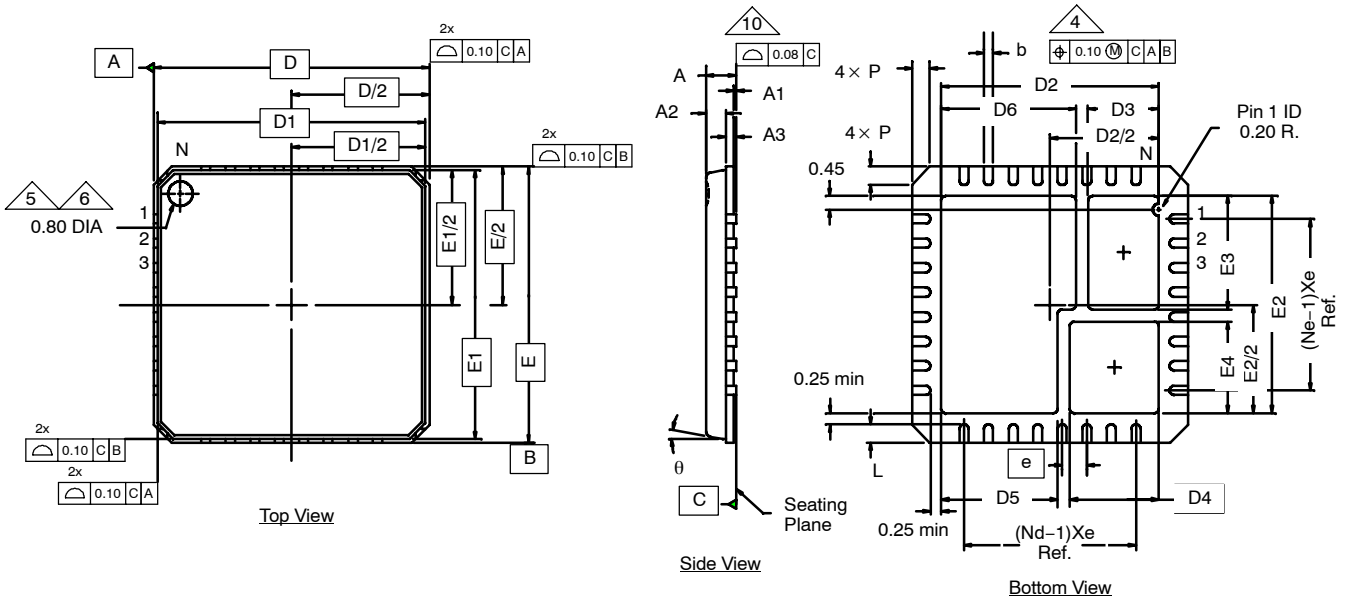
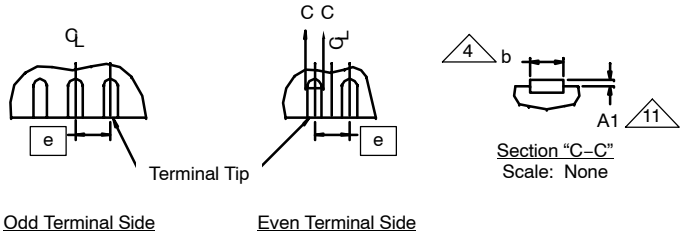



**Figure 8.**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73672.*

## PowerPAK® MLF 9×9




NOTES:

1. Die thickness allowable is 0.305-maximum (0.12-inches maximum)
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. N is the total number of terminals. Nd is the number of terminals in the X-direction and Ne is the number of terminals in the Y-direction.
4. Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from the terminal tip.
5. The pin #1 identifier must exist on the top surface of the package. The identifier may be an indentation mark or other feature of the package body.
6. Exact shape and size of this feature is optional.
7. Millimeters will govern.
8. The shape shown on four corners are not actual I/O.
9. Package warpage maximum is 0.08 mm.
10. Applied for exposed pad and terminals exclude embedding part of exposed pad from measuring.
11. Applied only for terminals.

### PowerPAK® MLF 9 × 9

| EXPOSED PAD VARIATIONS (Millimeters) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D2 | | | E2 | | | D3 | | | E3 | | |
| Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max |
| 6.95 | 7.10 | 7.25 | 6.95 | 7.10 | 7.25 | 2.15 | 2.30 | 2.45 | 3.55 | 3.70 | 3.85 |
| D4 | | | E4 | | | D5 | | | D6 | | |
| Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max |
| 2.75 | 2.90 | 3.05 | 2.85 | 3.00 | 3.15 | 3.65 | 3.80 | 3.95 | 4.25 | 4.40 | 4.55 |
| **EXPOSED PAD VARIATIONS (Inches)** | | | | | | | | | | | |
| D2 | | | E2 | | | D3 | | | E3 | | |
| Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max |
| 0.274 | 0.280 | 0.285 | 0.274 | 0.280 | 0.285 | 0.085 | 0.091 | 0.096 | 0.140 | 0.146 | 0.152 |
| D4 | | | E4 | | | D5 | | | D6 | | |
| Min | Nom | Max | Min | Nom | Max | Min | Nom | Max | Min | Nom | Max |
| 0.108 | 0.114 | 0.120 | 0.112 | 0.118 | 0.124 | 0.144 | 0.150 | 0.155 | 0.167 | 0.173 | 0.179 |

| DIMENSIONS | | | | | | | |
|---|---|---|---|---|---|---|---|
| | MILLIMETERS* | | | INCHES | | | |
| Dim | Min | Nom | Max | Min | Nom | Max | NOTE |
| A | — | 0.85 | 0.90 | — | 0.033 | 0.035 | |
| A1 | 0.00 | 0.01 | 0.05 | 0.000 | — | 0.002 | 11 |
| A2 | — | 0.65 | 0.80 | — | 0.026 | 0.031 | |
| A3 | | 0.20 REF | | | 0.008 REF | | |
| b | 0.25 | 0.30 | 0.35 | 0.010 | 0.012 | 0.014 | 4 |
| D | | 9.00 BSC | | | 0.354 BSC | | |
| D1 | | 8.75 BSC | | | 0.344 BSC | | |
| e | | 0.80 BSC | | | 0.031 BSC | | |
| E | | 9.00 BSC | | | 0.354 BSC | | |
| E1 | | 8.75 BSC | | | 0.344 BSC | | |
| L | 0.50 | 0.60 | 0.75 | 0.020 | 0.024 | 0.030 | |
| N | | 32 | | | 32 | | 3 |
| Nd | | 8 | | | 8 | | 3 |
| Ne | | 8 | | | 8 | | 3 |
| P | 0.24 | 0.42 | 0.60 | 0.009 | 0.017 | 0.024 | |
| θ | — | — | 12° | — | — | 12° | |

* Use millimeters as the primary measurement.

ECN: T-05143—Rev. A, 02-May-05
DWG: 5948

# Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Vishay products are not designed for use in life-saving or life-sustaining applications or any application in which the failure of the Vishay product could result in personal injury or death unless specifically qualified in writing by Vishay. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.