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Vishay Siliconix

Do

N-Channel MOSFET

Dual N-Channel 60 V (D-S) MOSFET

FEATURES

• 100 % Rg tested

APPLICATIONS

G.

ESD protected: 1800 V

• Material categorization:

Low power load switch

TrenchFET[®] power MOSFET

www.vishay.com/doc?99912

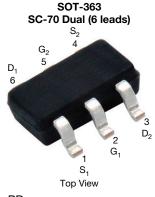
for definitions of compliance please see

D₁

S-

N-Channel MOSFET

PRODUCT SUMMARY							
V _{DS} (V)	R _{DS(on)} (Ω) MAX.	I _D (A)	Q _g (nC) TYP.				
60	1.4 at V _{GS} = 10 V	0.37	0.47				
	3 at V_{GS} = 4.5 V	0.25	0.47				



Marking Code: PD

Ordering Information: Si1926DL-T1-E3 (Lead (Pb)-free) Si1926DL-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	(T _A = 25 °C, unles	s otherwise no	oted)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	60	V	
Gate-Source Voltage		V _{GS}	± 20	V	
	T _C = 25 °C		0.37		
Continuous Drain Current (T. 150 °C)	T _C = 70 °C	°C	0.30	1	
Continuous Drain Current ($T_J = 150 \ ^{\circ}C$)	T _A = 25 °C	I _D	0.34 ^{b, c}	1	
	T _A = 70 °C		0.27 ^{b, c}	А	
Pulsed Drain Current		I _{DM}	0.65	1	
	T _C = 25 °C		0.43]	
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	0.25 ^{b, c}	1	
	T _C = 25 °C		0.51		
Mauinaum Dauca Diagingtian	T _C = 70 °C		0.33		
Maximum Power Dissipation	T _A = 25 °C	P _D	0.30 ^{b, c}	W	
	T _A = 70 °C	1	0.20 ^{b, c}	1	
Operating Junction and Storage Temperature F	T _J , T _{stg}	-55 to +150	°C		

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT			
Maximum Junction-to-Ambient b, d	t ≤ 5 s	R _{thJA}	360	415	°C (M)		
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	300	350	°C/W		

Notes

a. Based on $T_C = 25$ °C.

b. Surface mounted on 1" x 1" FR4 board.

c. t = 5 s.

d. Maximum under steady state conditions is 400 °C/W.

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Document Number: 73684



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PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT		
Static					·		
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \ \mu\text{A}$	60	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 050	-	56.7	-	m)//°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-3	-	mV/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	1	-	2.5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 10 V$	-	-	± 150	nA	
Zara Cata Valtaga Drain Current	I _{DSS}	$V_{DS} = 60 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1		
Zero Gate Voltage Drain Current		V _{DS} = 60 V, V _{GS} = 0 V, T _J = 85 °C		-	10	μΑ	
On Otata Duala Ourseat 3		$V_{DS} \ge 10 \text{ V}, V_{GS} = 4.5 \text{ V}$	0.50	-	-	— A	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 7.5 \text{ V}, V_{GS} = 10 \text{ V}$	0.65	-	-		
Drain Courses On State Desisters of	D	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 0.34 \text{ A}$	-	-	1.4	Ω	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 0.23 \text{ A}$	-	-	3		
Forward Transconductance	g _{fs}	$V_{DS} = 30 \text{ V}, \text{ I}_{D} = 0.2 \text{ A}$	-	159	-	ms	
Dynamic ^b				•			
Input Capacitance	C _{iss}		-	18.5	-	pF	
Output Capacitance	C _{oss}	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$	-	7.5	-		
Reverse Transfer Capacitance	C _{rss}		-	4.2	-		
Tabal Oaks Oksissa	Qg	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 0.34 \text{ A}$	-	0.9	1.4	nC	
Total Gate Charge			-	0.5	0.75		
Gate-Source Charge	Q _{gs}	$V_{DS} = 30$ V, $V_{GS} = 4.5$ V, $I_{D} = 0.34$ A	-	0.2	-		
Gate-Drain Charge	Q _{gd}		-	0.15	-		
Gate Resistance	R _g	f = 1 MHz	-	160	240	Ω	
Turn-On Delay Time	t _{d(on)}		-	6.5	10	- ns	
Rise Time	t _r	$V_{DD} = 30 \text{ V}, \text{ R}_{1} = 100 \Omega,$	-	12	18		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 0.3 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	13	22		
Fall Time	t _f		-	14	21		
Drain-Source Body Diode Characteris	tics						
Continuous Sorce-Drain Diode Current	I _S	T _C = 25 °C	-	-	0.43		
Pulse Diode Forward Current ^a	I _{SM}		-	-	0.65	A	
Body Diode Voltage	V _{SD}	I _S = 0.3 A	-	0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}		-	16.5	25	ns	
Body Diode Reverse Recovery Charge	Q _{rr}		-	13	20	nC	
Reverse Recovery Fall Time	$I_F = 0.6 \text{ A, dl/dt} = 100 \text{ A/}\mu\text{s}$		-	13.5	-		
Reverse Recovery Rise Time	t _b		-	3	-	ns	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

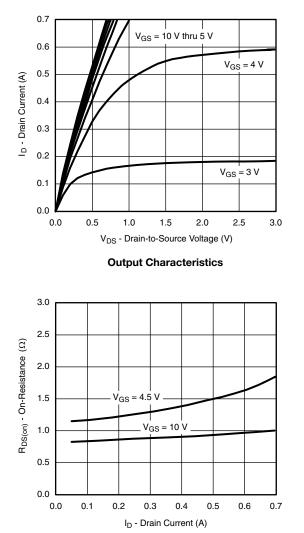
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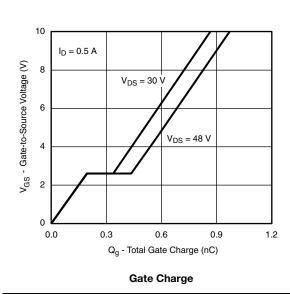


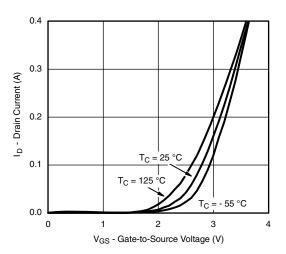
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TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

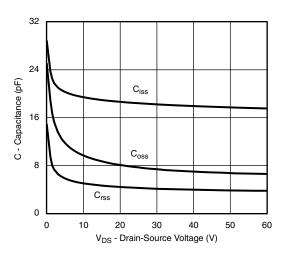




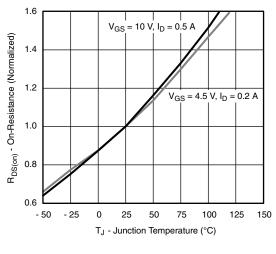




Transfer Characteristics Curves vs. Temperature







On-Resistance vs. Junction Temperature

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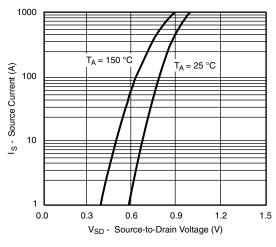
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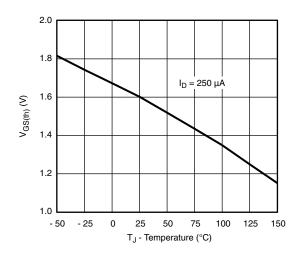


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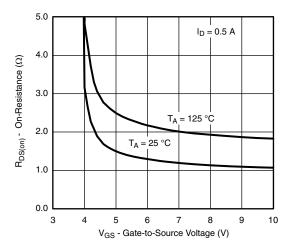
TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



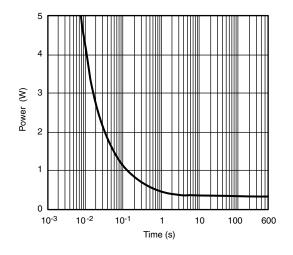
Source-Drain Diode Forward Voltage

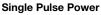


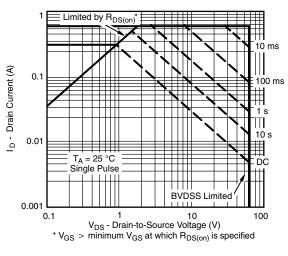
Threshold Voltage



R_{DS(on)} vs. V_{GS} vs. Temperature







Safe Operating Area 4

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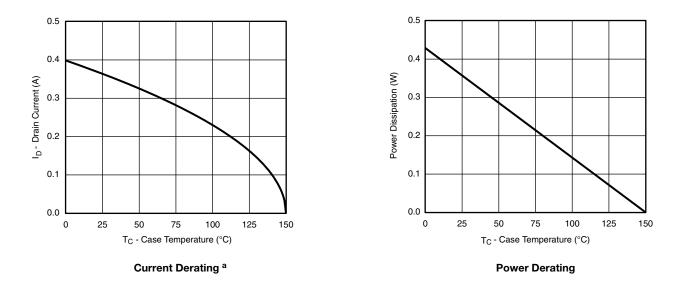
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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



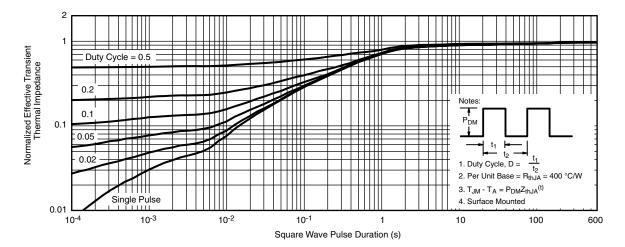
Note

a. The power dissipation P_D is based on T_{J (max.)} = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

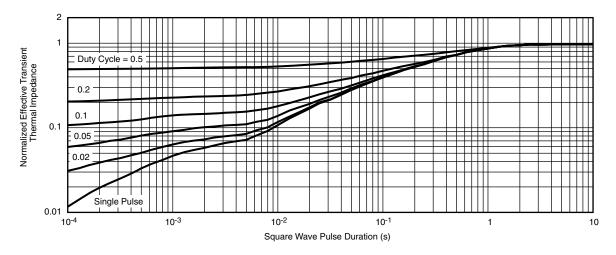


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TYPICAL CHARACTERISTICS ($T_A = 25 \text{ °C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73684.



Package Information Vishay Siliconix

SC-70: 6-LEADS





	MILLIMETERS			INCHES		
Dim	Min	Nom	Max	Min	Nom	Max
Α	0.90	-	1.10	0.035	-	0.043
A ₁	-	-	0.10	-	-	0.004
A ₂	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
С	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
Е	1.80	2.10	2.40	0.071	0.083	0.094
E ₁	1.15	1.25	1.35	0.045	0.049	0.053
е	0.65BSC			0.026BSC		
e ₁	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
٩	7°Nom			7°Nom		
ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5550						

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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