

Vishay Siliconix

P-Channel 1.8-V (G-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A) ^b	Q _g (Typ.)			
	0.009 at V _{GS} = - 4.5 V	- 13.7				
- 8	0.011 at V _{GS} = - 2.5 V	- 12.4	55 nC			
	0.016 at V _{GS} = - 1.8 V	- 10				

FEATURES

Halogen-free According to IEC 61249-2-21
Available

GO

- TrenchFET[®] Power MOSFET
- 1.8 V Rated
- 100 % Rg Tested



Ordering Information: Si4465ADY-T1-E3 (Lead (Pb)-free)





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ABSOLUTE MAXIMUM PATINGS T 25 °C unloss othorwis
Si4465ADY-T1-GE3 (Lead (Pb)-free and Halogen-free)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	- 8	V
Gate-Source Voltage		V _{GS}	± 8	
	T _A = 25 °C		- 13.7	
	T _A = 70 °C	-	- 11	
Continuous Drain Current (T _J = 150 °C) ^{a, b}	T _C = 25 °C	I _D	- 20	
	T _C = 70 °C		- 16	А
Pulsed Drain Current	I _{DM}	- 40	7	
Continuous Source Current (Diode Conduction) ^{a, b}		ا _S	- 2.5	
		I _{SM}	40	
Maximum Power Dissipation ^{a, b}	T _A = 25 °C		3.0	
	T _A = 70 °C	P _D	1.95	w
	T _C = 25 °C	' U	6.5	~~~~
	T _C = 70 °C		4.2	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
	t ≤ 10 s	R _{thJA}	34	41	°C/W	
Maximum Junction-to-Ambient (MOSFET) ^a	Steady State		67	80	0/10	
Maximum Junction-to-Foot (Drain)	Steady State	R _{thJF}	15	19		

Notes:

a. Surface Mounted on 1" x 1" FR4 board.

b. $t \leq$ 10 s.

SO-8 S D 8 1 D S 2 7 S D 6 3 D G 4 5 Top View

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	- 0.45		- 1.0	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 8 V$			± 100	nA	
Zara Cata Valtaga Drain Current	I _{DSS}	$V_{DS} = -8 V, V_{GS} = 0 V$ $V_{DS} = -8 V, V_{GS} = 0 V, T_{J} = 55 °C$			- 1	μA	
Zero Gate Voltage Drain Current					- 5		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge -5$ V, V_{GS} = -4.5 V	- 20			Α	
	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 14 A	0.0075 0.0		0.009		
Drain-Source On-State Resistance ^a		V _{GS} = - 2.5 V, I _D = - 12 A		0.0092	0.011	Ω	
		$V_{GS} = 1.8 \text{ V}, \text{ I}_{D} = 10 \text{ A}$		0.013	0.016		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 14 A		58		S	
Diode Forward Voltage ^a	V _{SD}	$I_{\rm S}$ = - 2.1 A, $V_{\rm GS}$ = 0 V		- 0.57	- 1.2	V	
Dynamic ^b						1	
Total Gate Charge	Qg			55	85		
Gate-Source Charge	Q _{gs}	V_{DS} = - 4 V, V_{GS} = - 4.5 V, I_{D} = - 14 A		6		nC	
Gate-Drain Charge	Q _{gd}		-	10		1	
Gate Resistance	Rg			2.5	3.8	Ω	
Turn-On Delay Time	t _{d(on)}			33	50		
Rise Time	t _r	V_{DD} = - 4 V, R_L = 4 Ω	-	170	255		
Turn-Off Delay Time	t _{d(off)}	$\text{I}_{\text{D}}\cong$ - 10 A, V_{GEN} = - 4.5 V, R_{g} = 6 Ω		168	255	ns	
Fall Time	t _f			112	170		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 2.1 A, dl/dt = 100 A/μs		85	130		
Body Diode Reverse Recovery Charge	Q _{rr}	$r_{\rm F} = -2.1$ A, $u/u_{\rm I} = 100$ A/µS		81	125	nC	

Notes:

a. Pulse test; pulse width \leq 300 $\mu s,$ duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

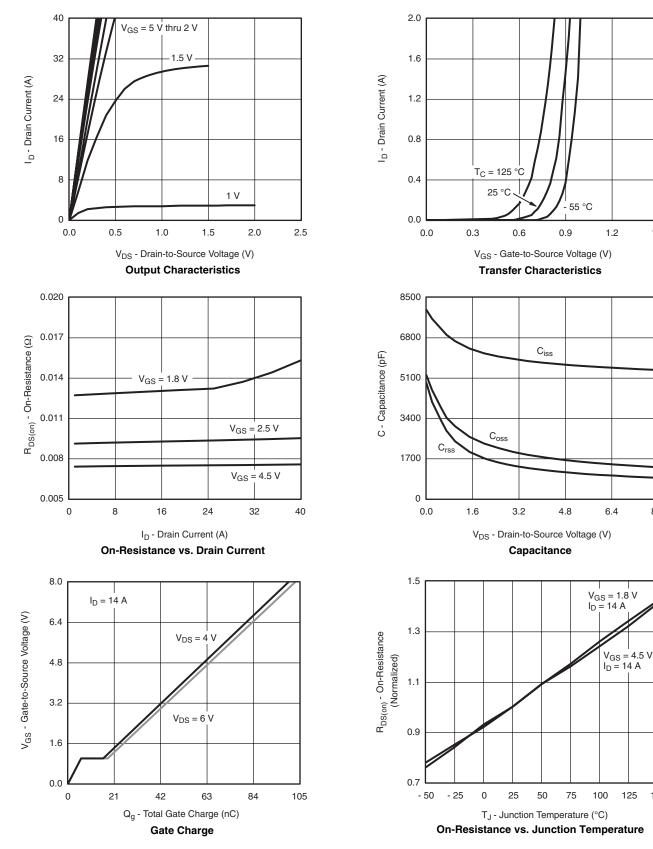


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1.5

8.0

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



125

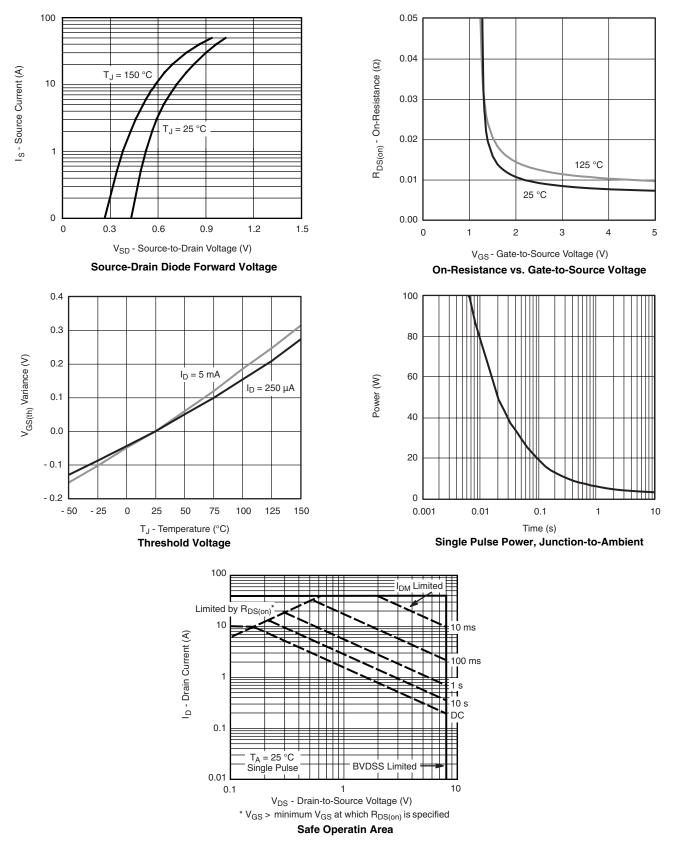
150

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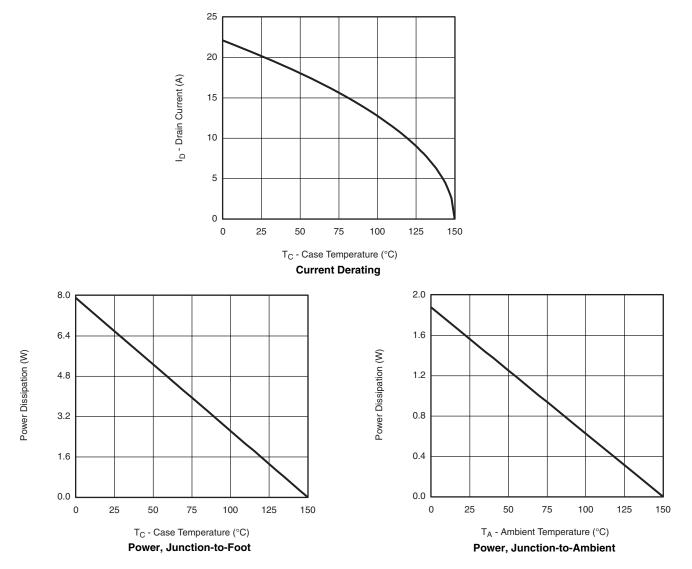
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



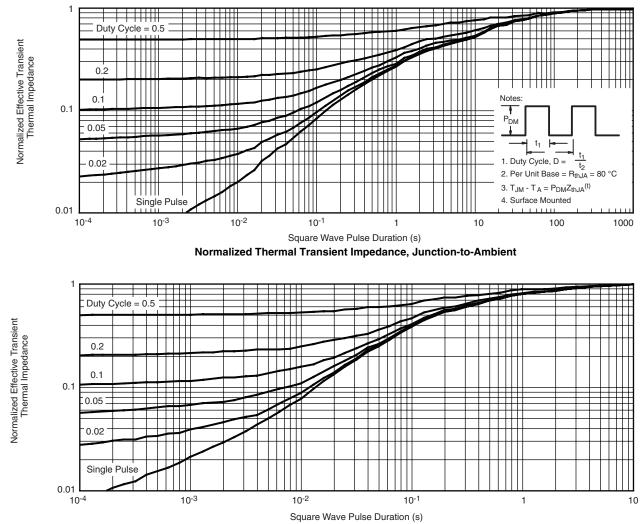
* The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?73856.



Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES			
DIM	Min	Мах	Min	Max		
A	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
E	3.80	4.00	0.150	0.157		
е	1.27	BSC	0.050 BSC			
н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498						

Application Note 826

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RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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