



N- and P-Channel 40-V (D-S) MOSFET

CHARACTERISTICS

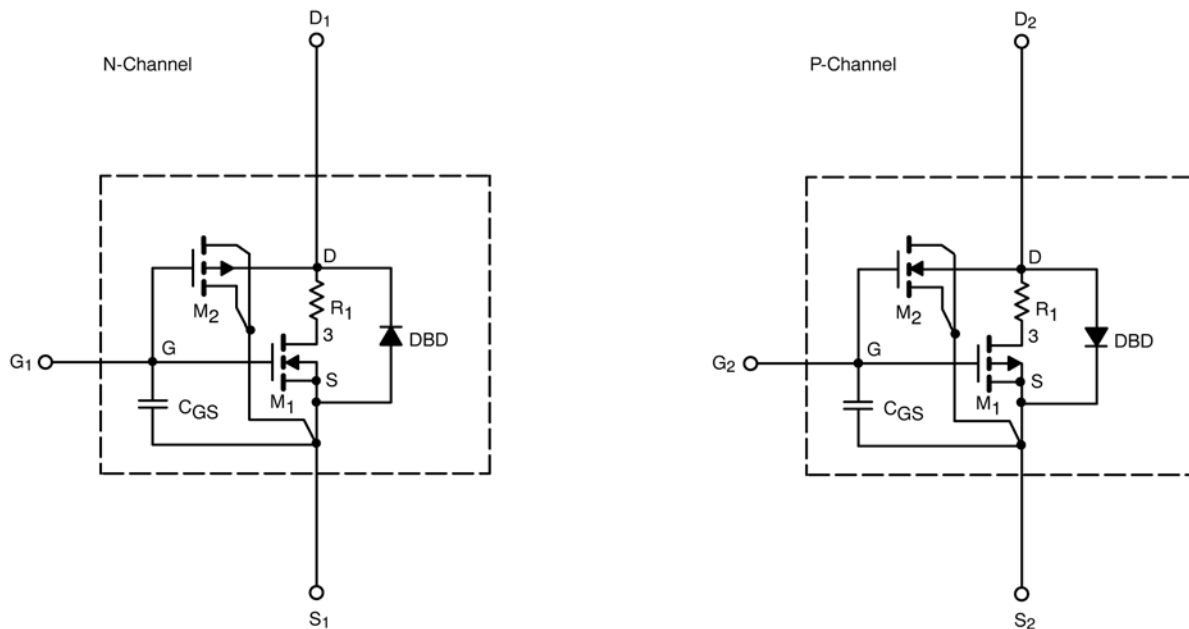
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition		Simulated Data	Measured Data	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	N-Ch	1.1		
		$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	P-Ch	1.6		
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	N-Ch	365		A
		$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	P-Ch	240		
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	N-Ch	0.013	0.013	Ω
		$V_{GS} = -10 \text{ V}, I_D = -5 \text{ A}$	P-Ch	0.020	0.020	
		$V_{GS} = 4.5 \text{ V}, I_D = 4 \text{ A}$	N-Ch	0.015	0.015	
		$V_{GS} = -4.5 \text{ V}, I_D = -4 \text{ A}$	P-Ch	0.025	0.025	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}, I_D = 5 \text{ A}$	N-Ch	36	23	S
		$V_{DS} = -15 \text{ V}, I_D = -5 \text{ A}$	P-Ch	19	18	
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.5 \text{ A}$	N-Ch	0.71	0.69	V
		$I_S = -1.5 \text{ A}$	P-Ch	-0.80	-0.72	
Dynamic^b						
Total Gate Charge	Q_g	N-Channel $V_{DS} = 20 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$ P-Channel $V_{DS} = -20 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -5 \text{ A}$	N-Ch	25	26	nC
Gate-Source Charge	Q_{gs}		P-Ch	25	25.5	
			N-Ch	5.5	5.5	
Gate-Source Charge	Q_{gs}		P-Ch	5.1	5.1	
			N-Ch	9.7	9.7	
			P-Ch	11.7	11.7	

Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

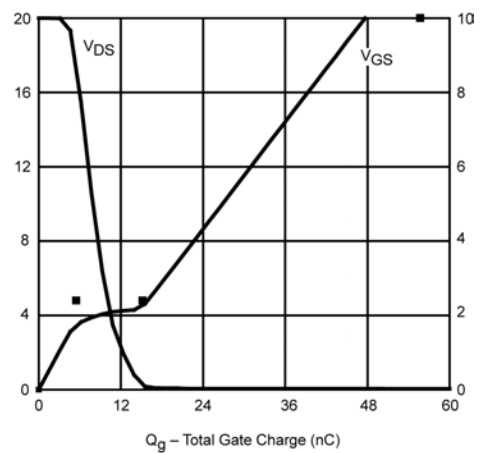
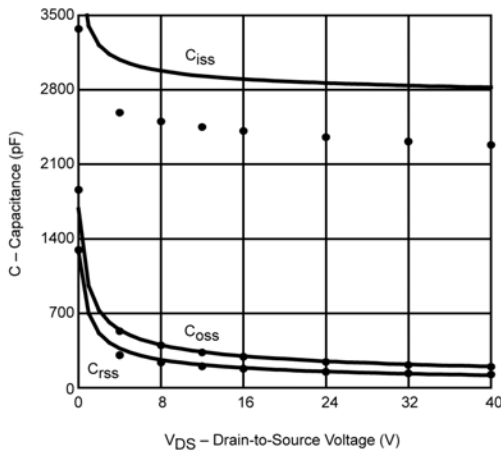
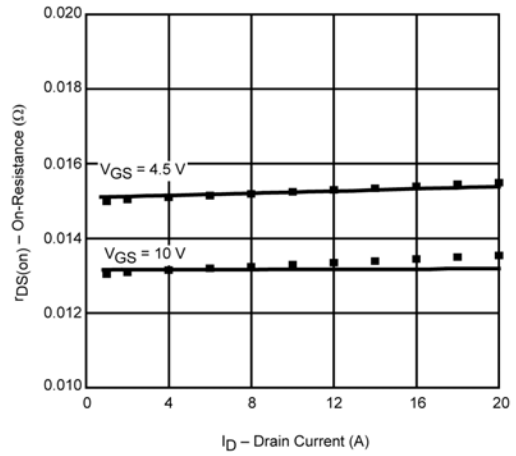
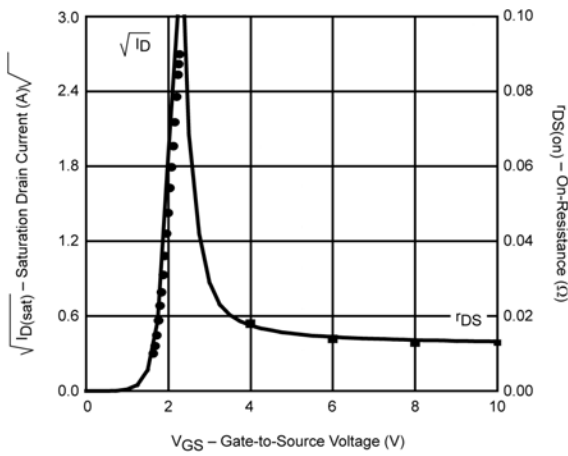
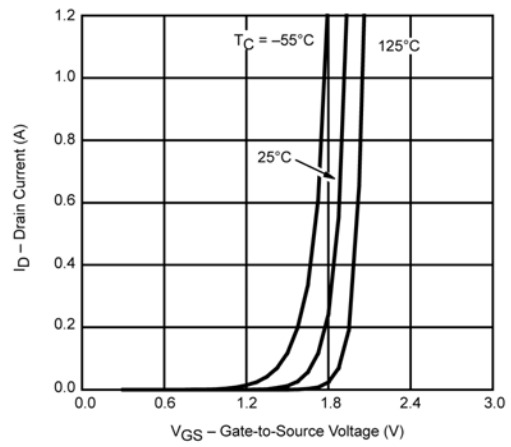
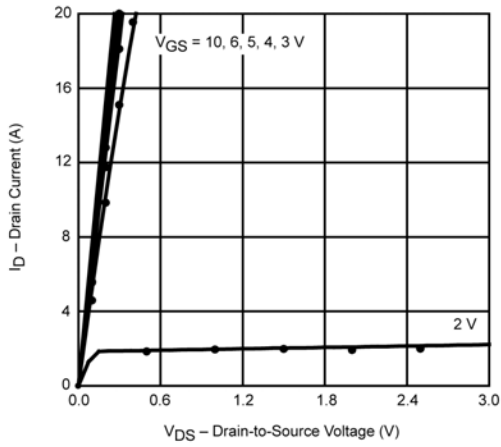


SPICE Device Model Si4563DY

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COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

N-Channel MOSFET



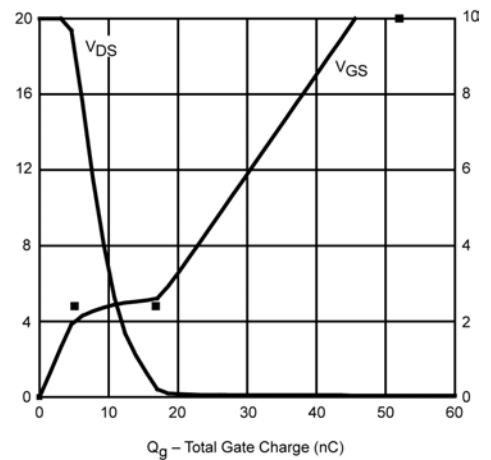
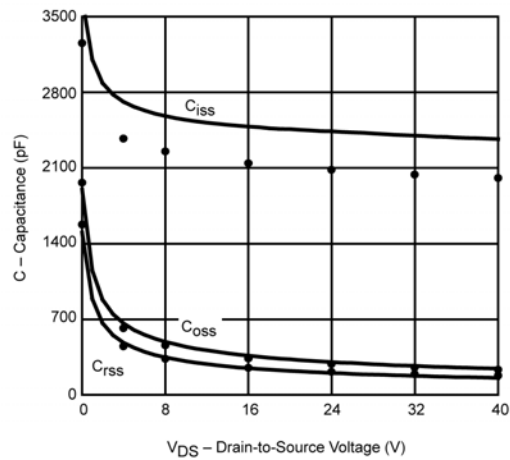
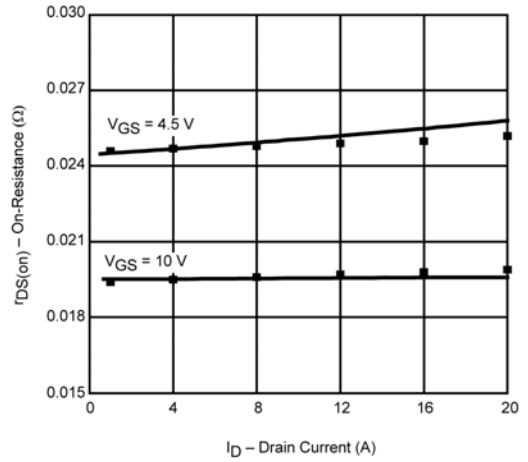
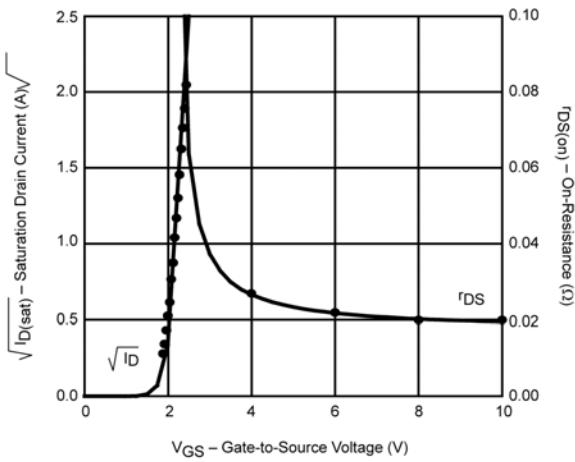
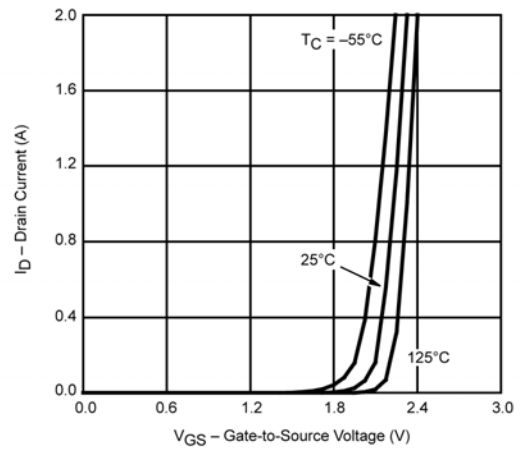
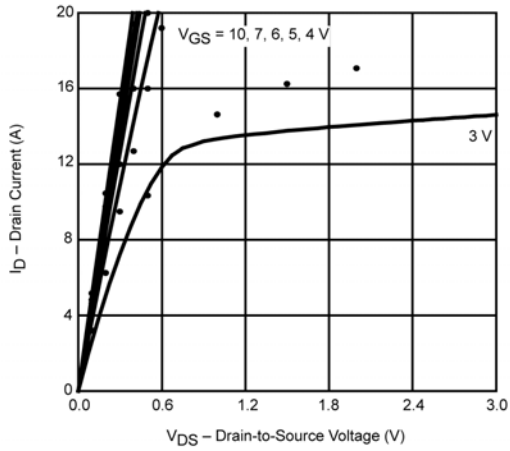
Note: Dots and squares represent measured data.

SPICE Device Model Si4563DY

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P-Channel MOSFET



Note: Dots and squares represent measured data.



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