Dual N- and P-Channel 40-V (D-S) MOSFET

CHARACTERISTICS

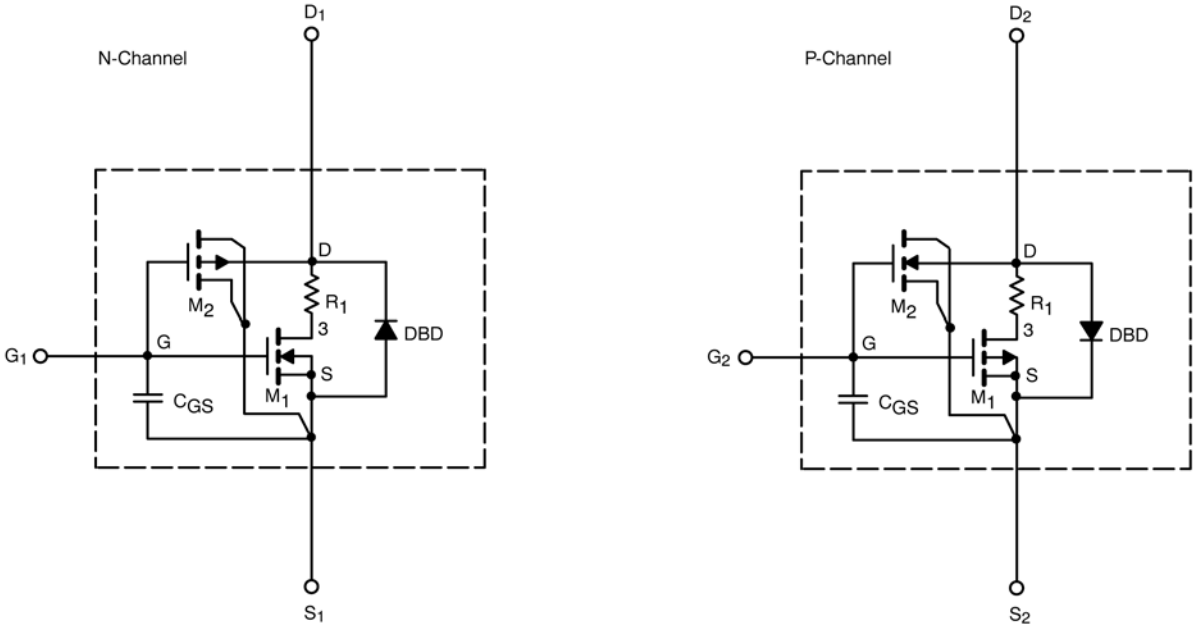
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



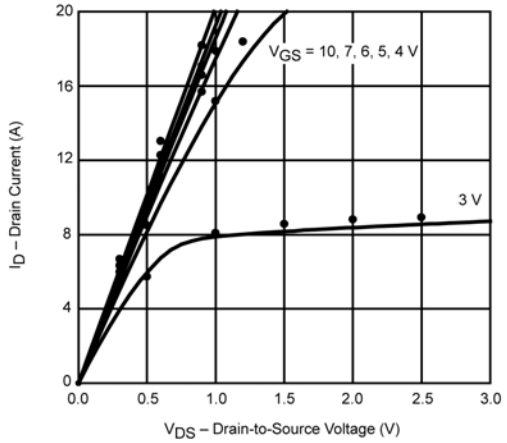
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

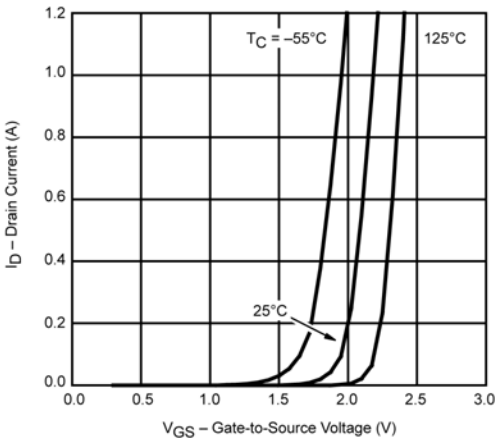
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)						
Parameter	**Symbol**	**Test Condition**		**Simulated Data**	**Measured Data**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	N-Ch	1.4		V
		V_{DS} = V_{GS}, I_D = –250 μA	P-Ch	1.9		
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	N-Ch	97		A
		V_{DS} = –5 V, V_{GS} = –10 V	P-Ch	67		
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 4.1 A	N-Ch	0.049	0.048	Ω
		V_{GS} = –10 V, I_D = –3.6 A	P-Ch	0.056	0.058	
		V_{GS} = 4.5 V, I_D = 3.8 A	N-Ch	0.056	0.056	
		V_{GS} = –4.5 V, I_D = –2.9 A	P-Ch	0.097	0.097	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 4.1 A	N-Ch	9	15	S
		V_{DS} = –15 V, I_D = –3.6 A	P-Ch	6.3	7	
Diode Forward Voltage[a]	V_{SD}	I_S = 1.5 A, V_{GS} = 0 V	N-Ch	0.72	0.80	V
		I_S = –1.6 A, V_{GS} = 0 V	P-Ch	0.80	–0.80	
Dynamic[b]						
Input Capacitance	C_{ISS}	N-Channel V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = – 20 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	471	355	pF
			P-Ch	567	480	
Output Capacitance	C_{OSS}		N-Ch	53	50	
			P-Ch	76	80	
Reverse Transfer Capacitance	C_{RSS}		N-Ch	25	29	
			P-CH	57	56	
Total Gate Charge	Q_g	V_{DS} = 20 V, V_{GS} = 10 V, I_D = 5 A	N-Ch	6.5	8	nC
		V_{DS} = – 20 V, V_{GS} = –10 V, I_D = – 5 A	P-Ch	10.5	12	
		N-Channel V_{DS} = 20 V, V_{GS} = 4.5 V, I_D = 5 A P-Channel V_{DS} = – 20 V, V_{GS} = –4.5 V, I_D = – 5 A	N-Ch	3.3	3.7	
			P-Ch	5.7	6	
Gate-Source Charge	Q_{gs}		N-Ch	1.1	1.1	
			P-Ch	1.5	1.5	
Gate-Source Charge	Q_{gs}		N-Ch	1.4	1.4	
			P-Ch	2.7	2.7	

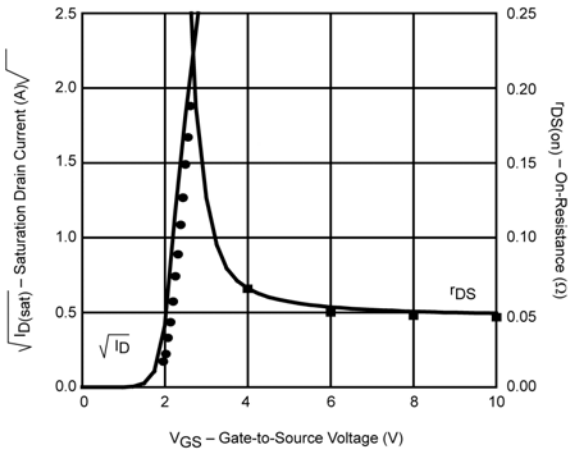
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

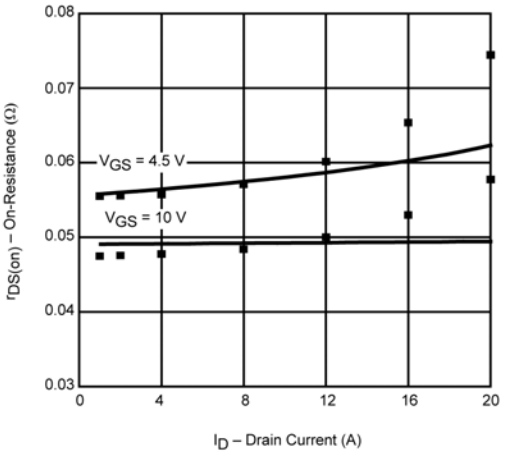
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

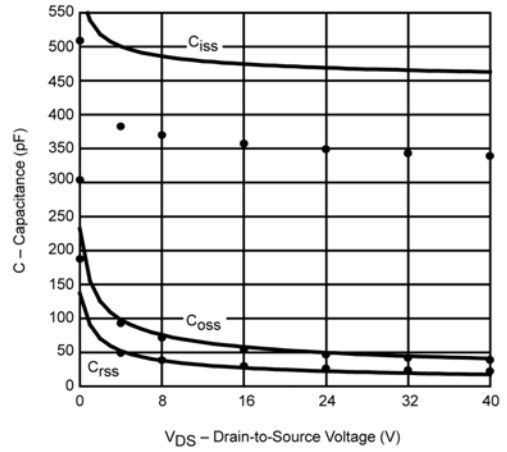
N-Channel MOSFET

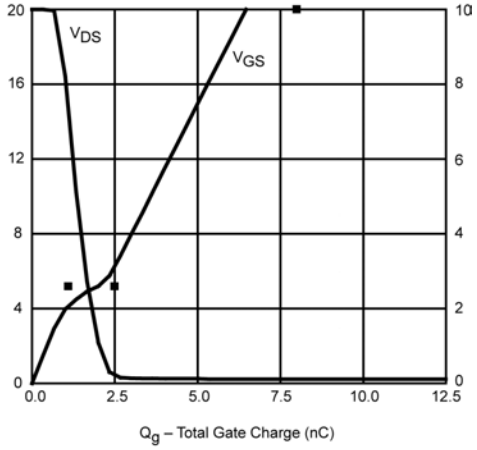






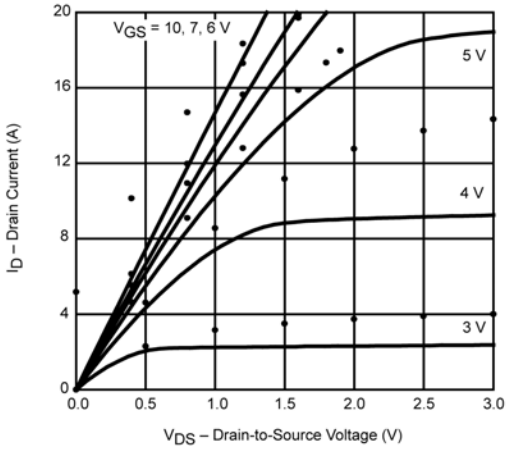


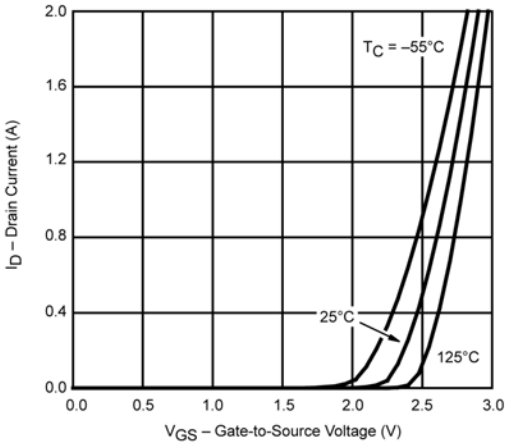


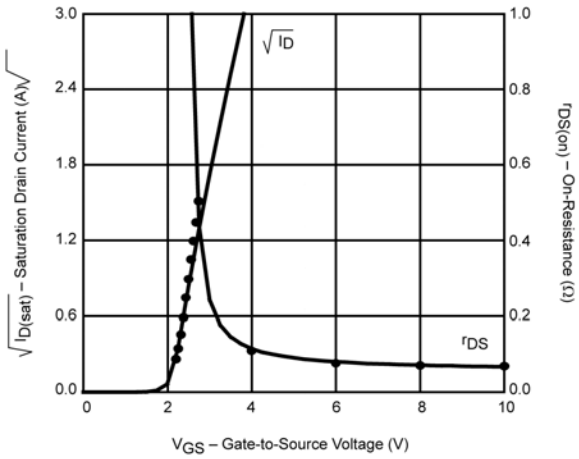


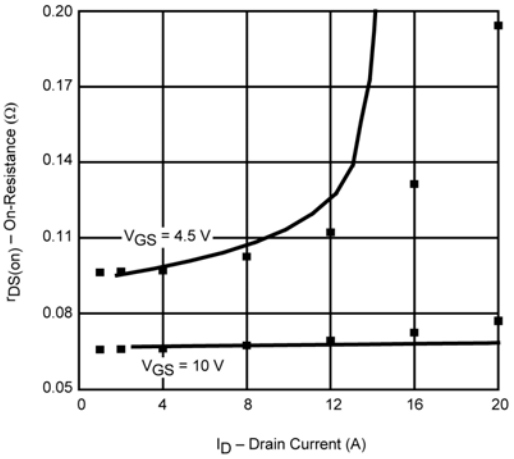
Note: Dots and squares represent measured data.

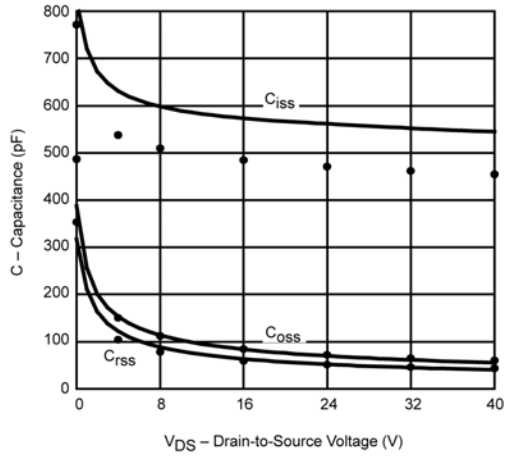
P-Channel MOSFET

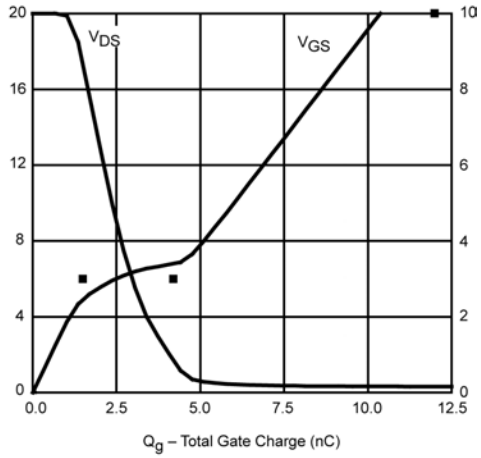












Note: Dots and squares represent measured data.

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