



N-Channel 12-V (D-S) MOSFET

CHARACTERISTICS

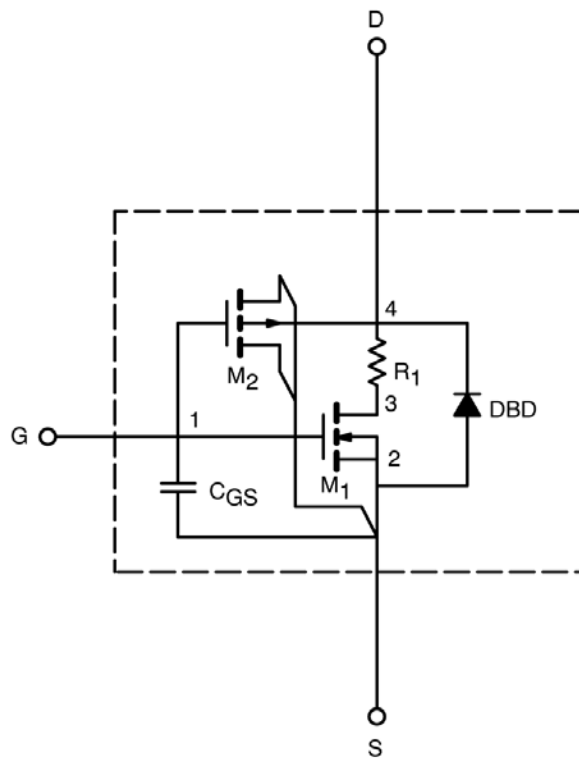
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	0.85		V
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5V, V _{GS} = 4.5V	1068		A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5V, I _D = 29A	0.0020	0.0020	Ω
		V _{GS} = 2.5V, I _D = 23A	0.0028	0.0029	
Forward Transconductance ^a	g _{fs}	V _{DS} = 6V, I _D = 29A	323	130	S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.9A, V _{GS} = 0V	0.76	0.75	V
Dynamic^b					
Total Gate Charge	Q _g	V _{DS} = 6V, V _{GS} = 4.5V, I _D = 29A	53	54	nC
Gate-Source Charge	Q _{gs}		10	10	
Gate-Drain Charge	Q _{gd}		16	16	

Notes

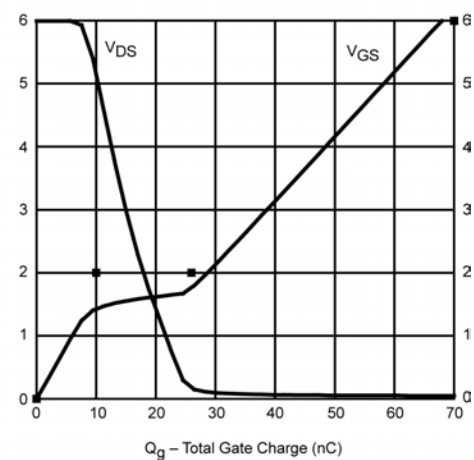
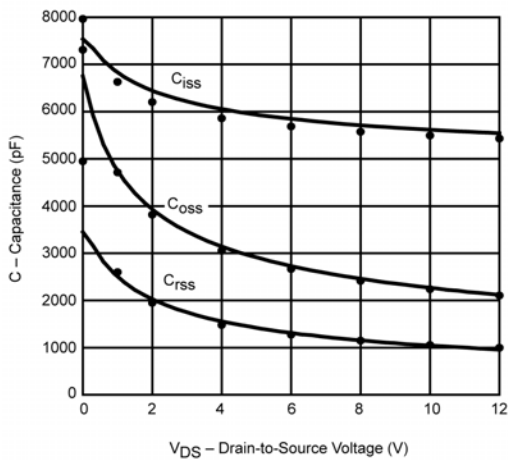
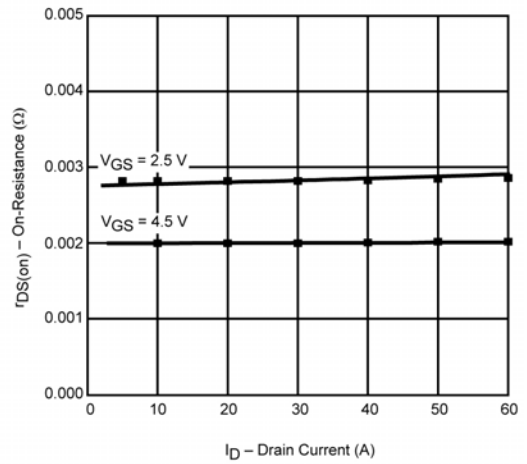
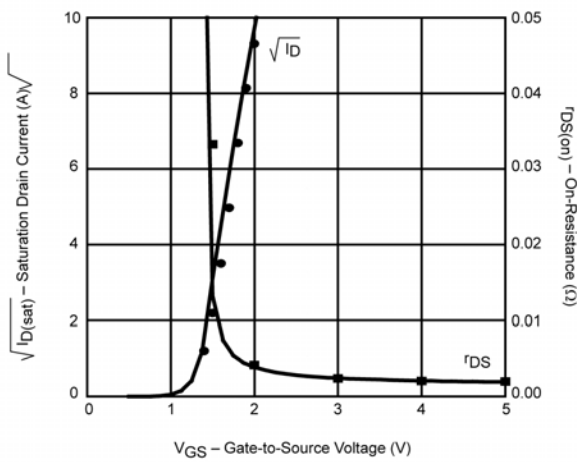
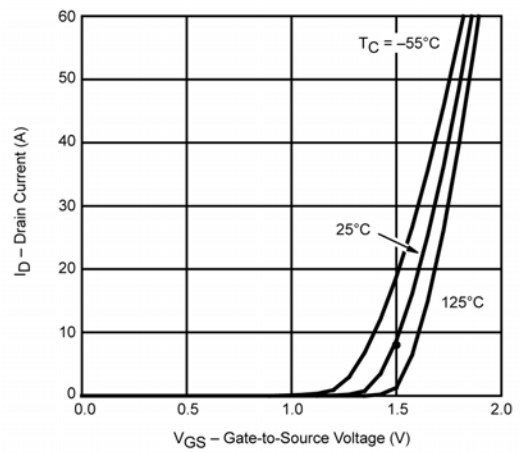
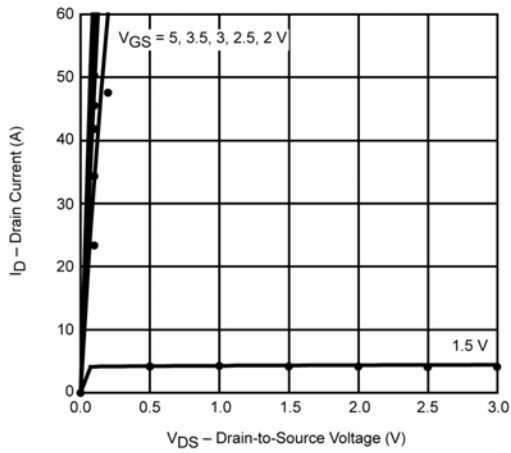
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



SPICE Device Model Si7858ADP

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



Disclaimer

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