Automotive N- and P-Channel 100 V (D-S) 175 °C MOSFET

DESCRIPTION

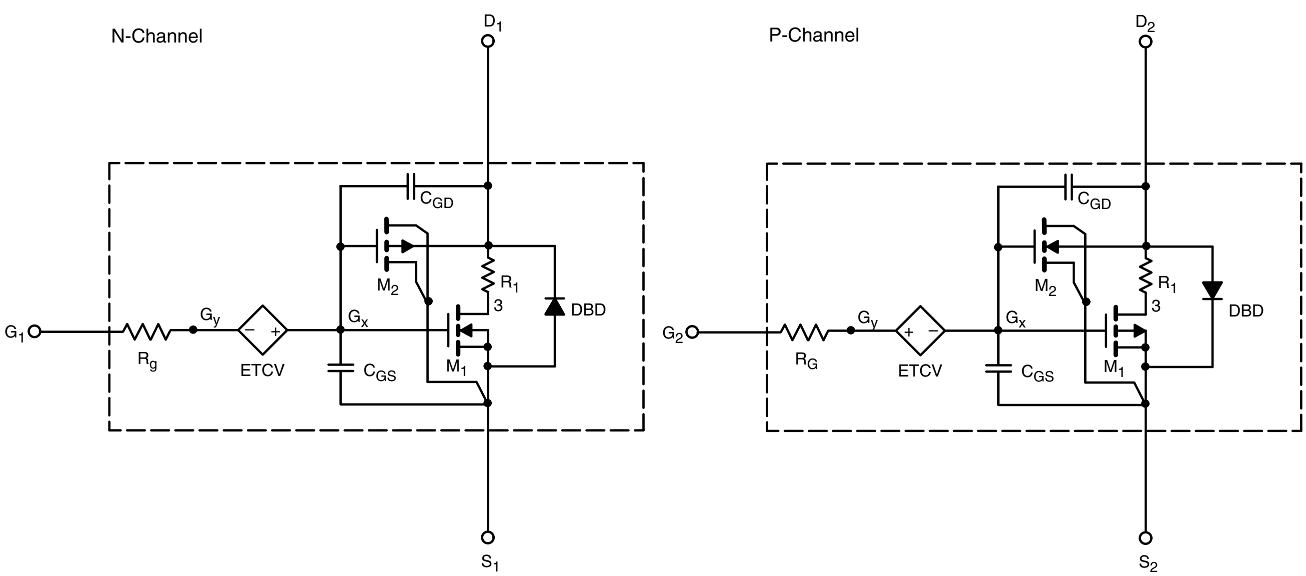
The attached SPICE model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N- and P-Channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	N-Ch	2	2	V
		$V_{DS} = V_{GS}$, I_D = -250 μA	P-Ch	2	2	
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 6 A	N-Ch	0.0351	0.0365	Ω
		V_{GS} = -10 V, I_D = -6 A	P-Ch	0.1233	0.1184	
		V_{GS} = 4.5 V, I_D = 4 A	N-Ch	0.0510	0.0468	
		V_{GS} = -4.5 V, I_D = -4 A	P-Ch	0.1800	0.1669	
Forward Transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 6 A	N-Ch	13	15	S
		V_{DS} = -15 V, I_D = -6 A	P-Ch	7.2	7	
Diode Forward Voltage [a]	V_{SD}	I_S = 6 A	N-Ch	0.86	0.89	V
		I_S = -6 A	P-Ch	-0.86	-0.89	
Dynamic [b]						
Input Capacitance	C_{iss}	N-Channel V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz P-Channel V_{DS} = -25 V, V_{GS} = 0 V, f = 1 MHz	N-Ch	450	420	pF
			P-Ch	588	480	
Output Capacitance	C_{oss}		N-Ch	260	260	
			P-Ch	240	250	
Reverse Transfer Capacitance	C_{rss}		N-Ch	16	17	
			P-Ch	29	20	
Total Gate Charge	Q_g	N-Channel V_{DS} = 50 V, V_{GS} = 10 V, I_D = 1 A P-Channel V_{DS} = -50 V, V_{GS} = -10 V, I_D = -1 A	N-Ch	8	9	nC
			P-Ch	10.2	12	
Gate-Source Charge	Q_{gs}		N-Ch	1.2	1.2	
			P-Ch	1.7	2	
Gate-Drain Charge	Q_{gd}		N-Ch	1.8	1.9	
			P-Ch	3.3	3	

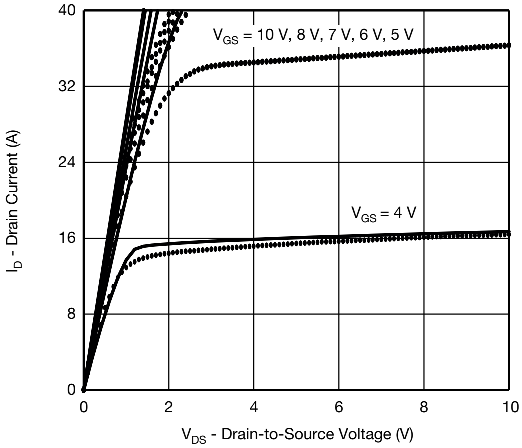
Notes

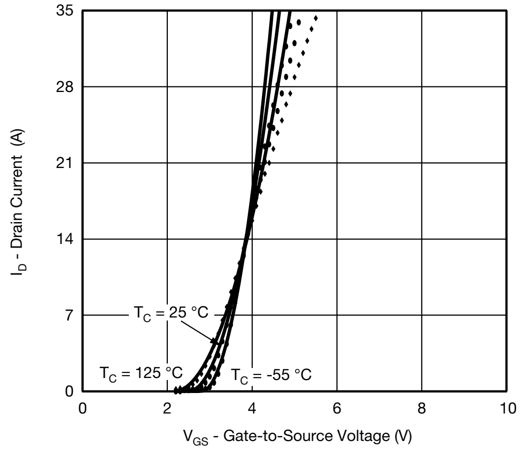
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %

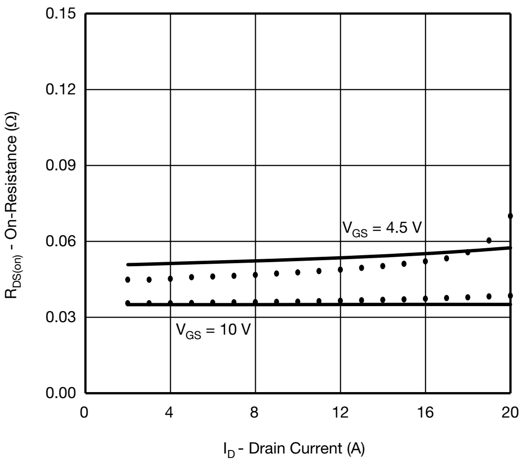
b. Guaranteed by design, not subject to production testing

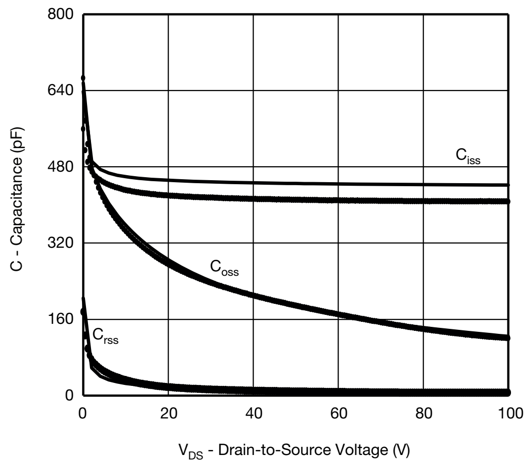
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

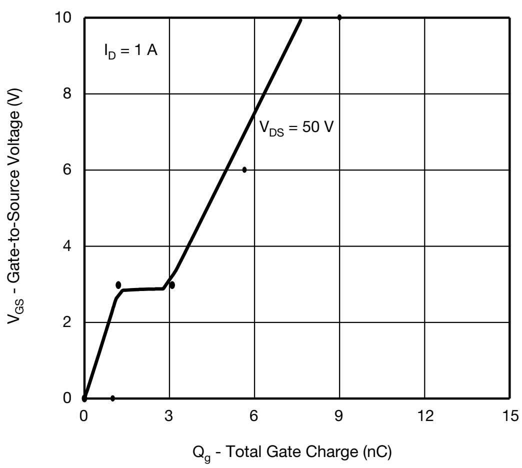
N-Channel MOSFET

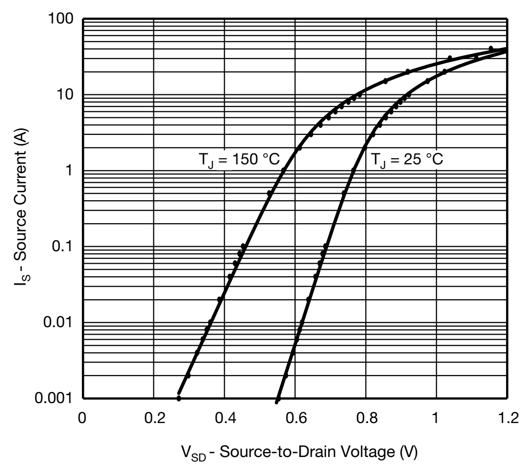










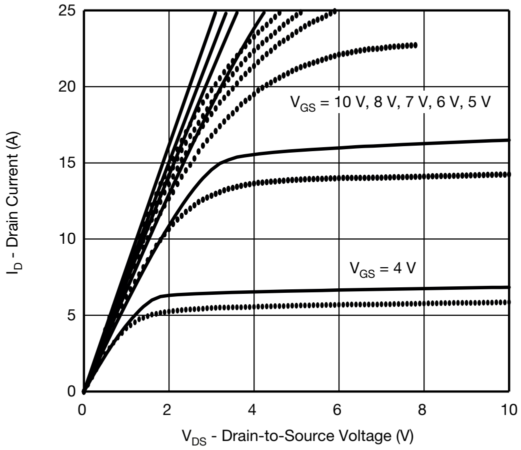


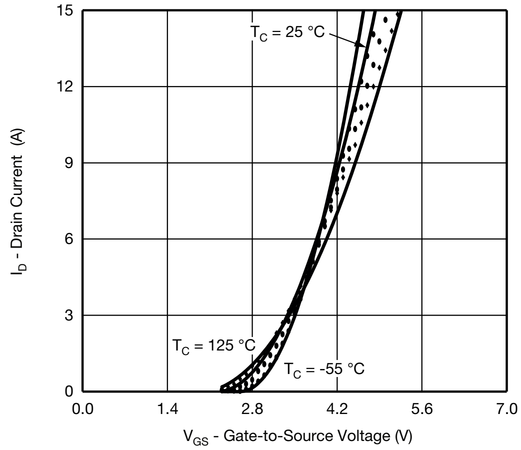
Note

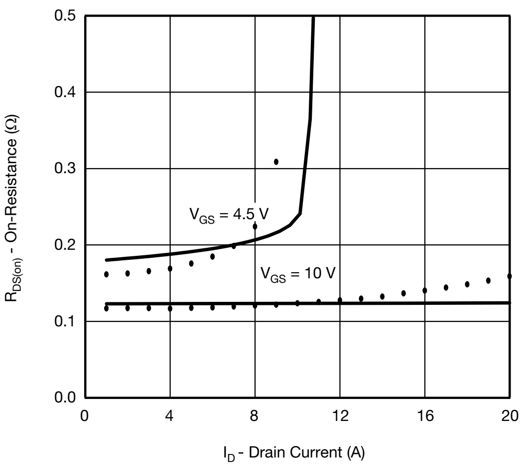
- Dots and squares represent measured data.

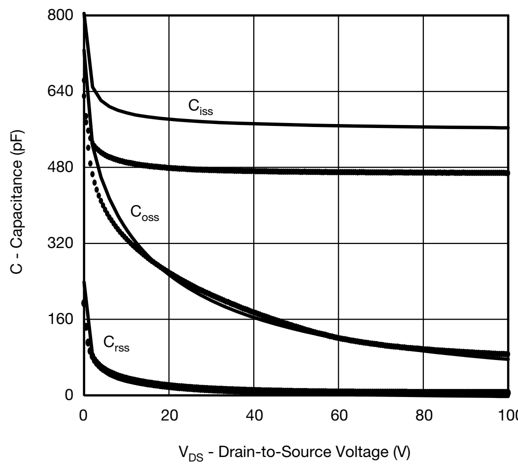
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

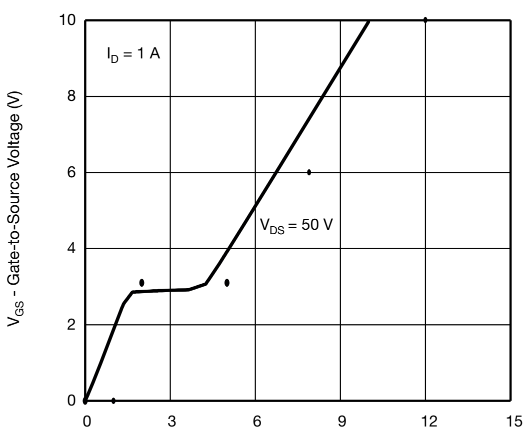
P-Channel MOSFET

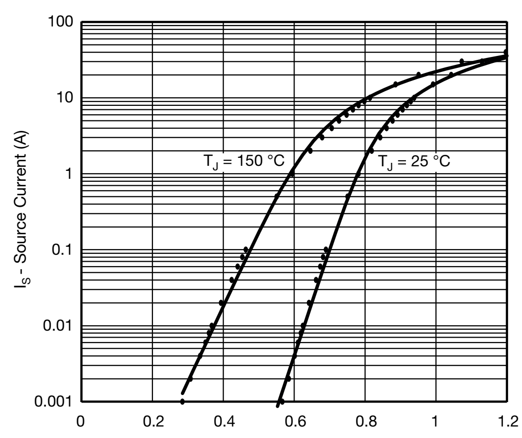












Note

- Dots and squares represent measured data.

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