

## P-Channel 20 V (D-S) MOSFET

### DESCRIPTION

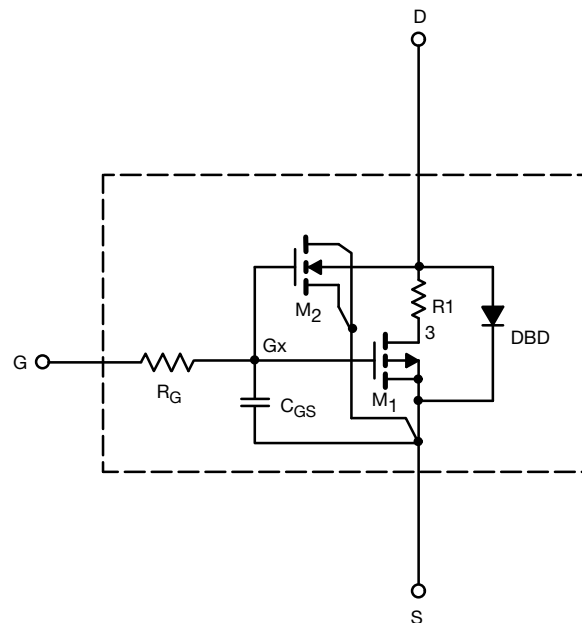
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 to 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics.

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



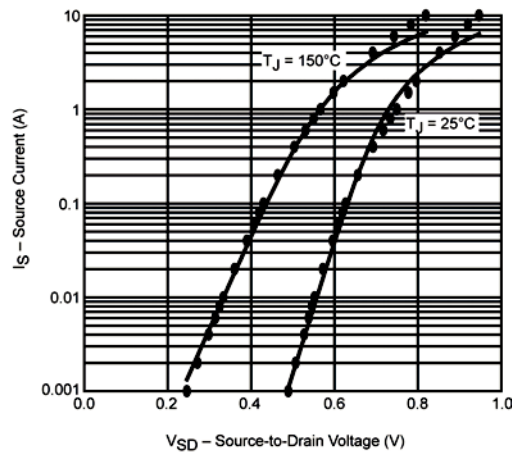
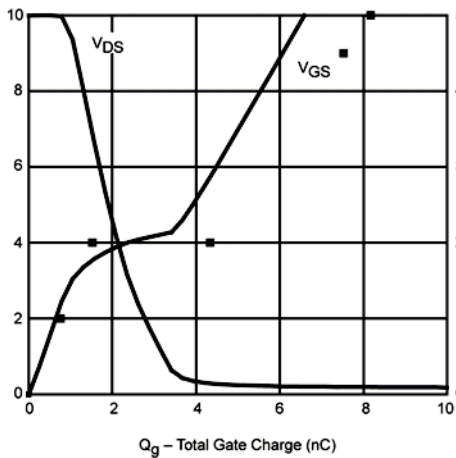
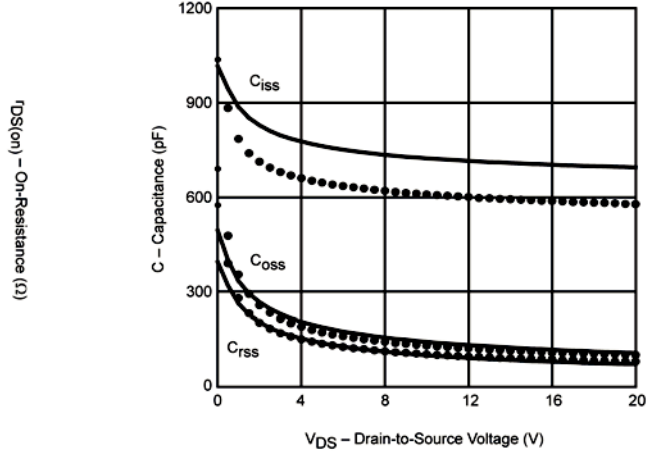
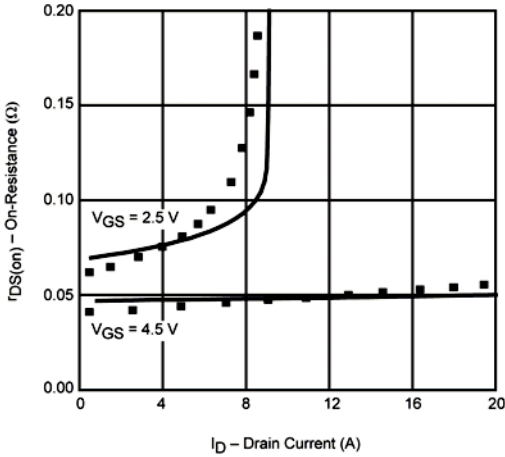
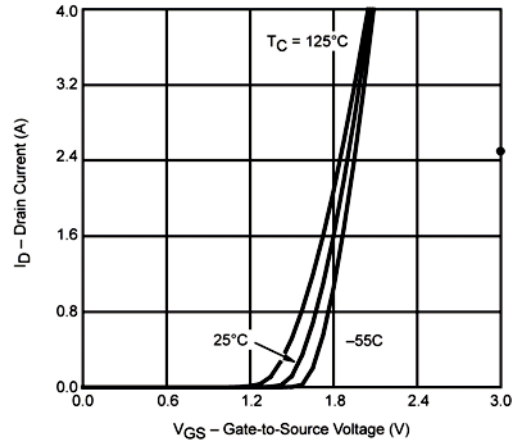
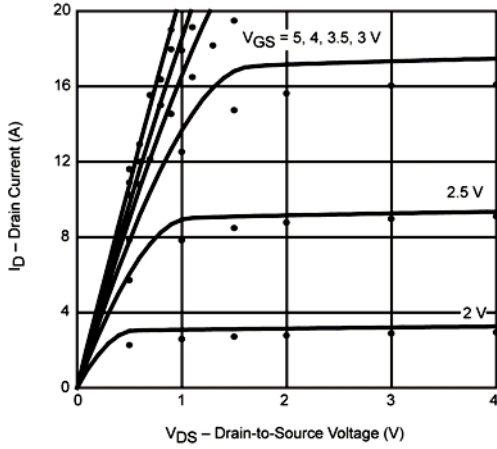
| <b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted) |              |  |                |               |          |
|--|--------------|--|----------------|---------------|----------|
| PARAMETER  | SYMBOL       | TEST CONDITION   | SIMULATED DATA | MEASURED DATA | UNIT     |
| <b>Static</b>  |              |  |                |               |          |
| Gate Threshold Voltage   | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$                     | 1.2            | -             | V        |
| On-State Drain Current <sup>a</sup>  | $I_{D(on)}$  | $V_{DS} \leq -5\text{ V}, V_{GS} = -4.5\text{ V}$                    | 50             | -             | A        |
| Drain-Source On-State Resistance <sup>a</sup>                                      | $R_{DS(on)}$ | $V_{GS} = -4.5\text{ V}, I_D = -4.7\text{ A}$                        | 0.048          | 0.050         | $\Omega$ |
|  |              | $V_{GS} = -2.5\text{ V}, I_D = -3.4\text{ A}$                        | 0.075          | 0.083         |          |
| Forward Transconductance <sup>a</sup>  | $g_{fs}$     | $V_{DS} = -10\text{ V}, I_D = -4.7\text{ A}$                         | 12             | 15            | S        |
| Diode Forward Voltage <sup>a</sup>   | $V_{SD}$     | $I_S = -1.7\text{ A}$  | -0.77          | -0.80         | V        |
| <b>Dynamic<sup>b</sup></b>   |              |  |                |               |          |
| Input Capacitance  | $C_{iss}$    | $V_{GS} = 0\text{ V}, V_{DS} = -10\text{ V}, f = 1\text{ MHz}$       | 724            | 610           | pF       |
| Output Capacitance   | $C_{oss}$    |  | 143            | 132           |          |
| Reverse Transfer Capacitance   | $C_{rss}$    |  | 101            | 105           |          |
| Total Gate Charge  | $Q_g$        | $V_{DS} = -10\text{ V}, V_{GS} = -5\text{ V}, I_D = -4.7\text{ A}$   | 6.7            | 8.26          | nC       |
| Gate-Source Charge   | $Q_{gs}$     | $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -4.7\text{ A}$ | 6.1            | 7.53          |          |
| Gate-Drain Charge <sup>c</sup>   | $Q_{gd}$     |  | 1.53           | 1.53          |          |
|  |              |  | 2.37           | 2.37          |          |

**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data.



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