



### P-Channel 8-V (D-S) MOSFET

#### CHARACTERISTICS

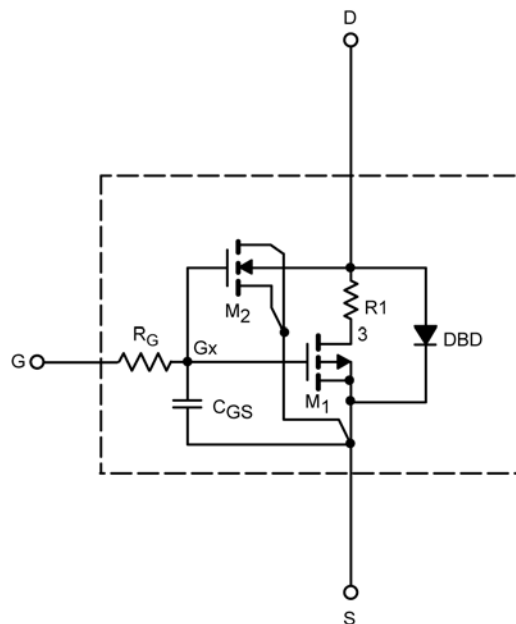
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model SiA417DJ



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SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
<b>Static</b>					
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	0.61		V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5 V, V <sub>GS</sub> = -4.5 V	192		A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -7 A	0.019	0.019	Ω
		V <sub>GS</sub> = -2.5 V, I <sub>D</sub> = -6 A	0.025	0.026	
		V <sub>GS</sub> = -1.8 V, I <sub>D</sub> = -5.3 A	0.034	0.033	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -4 V, I <sub>D</sub> = -7 A	38	23	S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = -8.3 A	-0.96	-0.80	V
<b>Dynamic<sup>b</sup></b>					
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -4 V, V <sub>GS</sub> = 0 V, f = 1 MHz	1758	1600	pF
Output Capacitance	C <sub>oss</sub>		487	500	
Reverse Transfer Capacitance	C <sub>rss</sub>		340	320	
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = -4 V, V <sub>GS</sub> = -5 V, I <sub>D</sub> = -10 A	14.4	21	nC
		V <sub>DS</sub> = -4 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -10 A	13.3	19	
Gate-Source Charge	Q <sub>gs</sub>		2.2	2.2	
Gate-Drain Charge	Q <sub>gd</sub>		5	5	

**Notes**

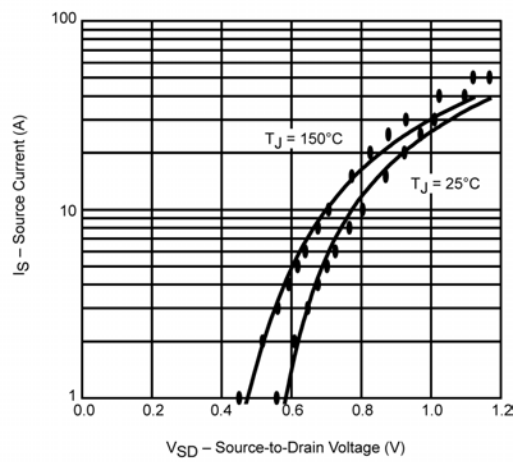
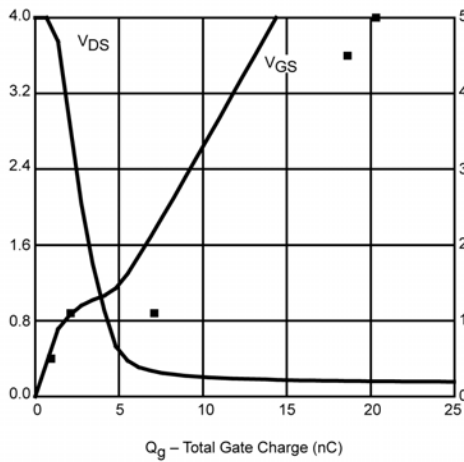
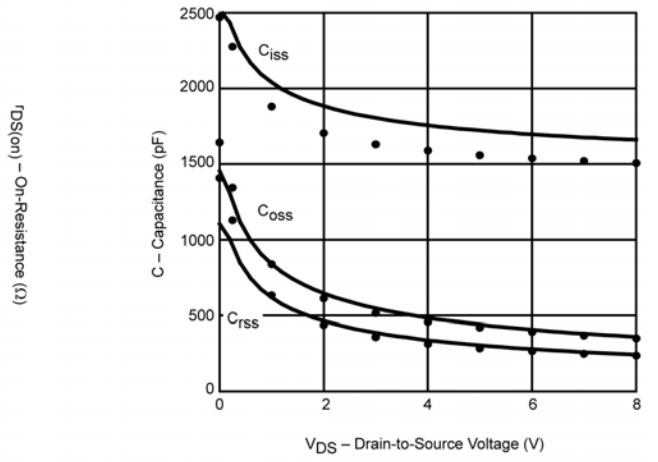
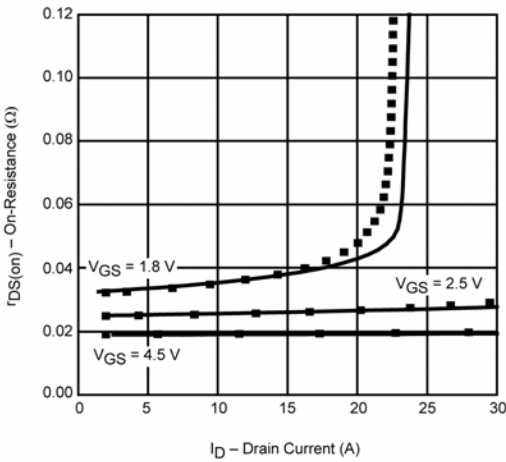
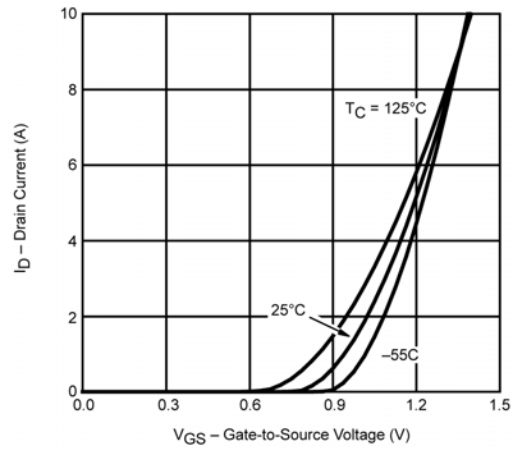
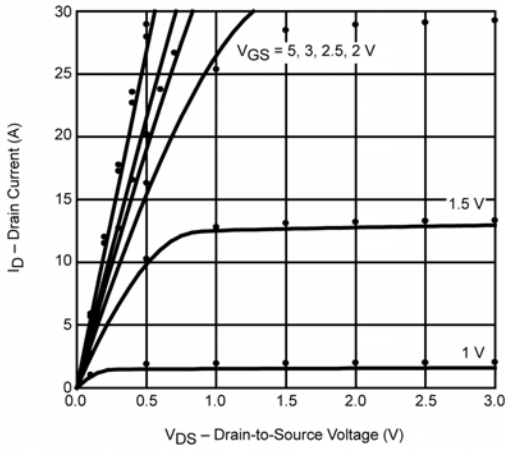
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.



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COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



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