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# Automotive N-Channel 40 V (D-S) 175 °C MOSFET

### **DESCRIPTION**

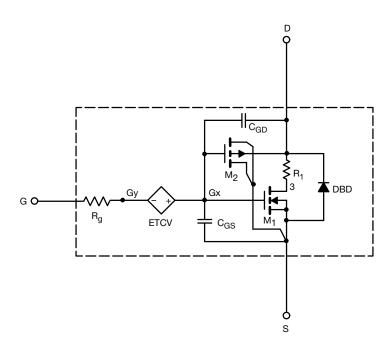
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{\rm gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### **CHARACTERISTICS**

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- · Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



## Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	3	V
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 35 A	0.00131	0.00133	Ω
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 35 A	201	143	S
Diode forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 60 A	0.82	0.83	V
Dynamic <sup>b</sup>					
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1 MHz	7100	6783	pF
Output capacitance	C <sub>oss</sub>		2010	1771	
Reverse transfer capacitance	C <sub>rss</sub>		161	109	
Total gate charge	Qg		104	106	
Gate-source charge	Q <sub>gs</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 100 \text{ A}$	33	33	nC
Gate-drain charge	Q <sub>gd</sub>		21	21	

#### Notes

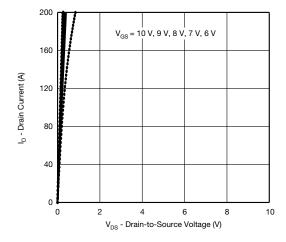
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing

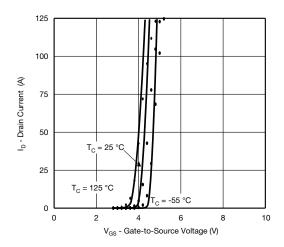


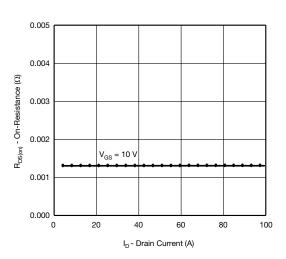
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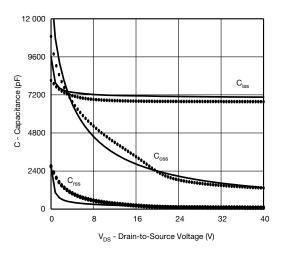
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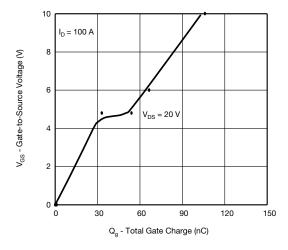
## **COMPARISON OF MODEL WITH MEASURED DATA** ( $T_J = 25$ °C, unless otherwise noted)

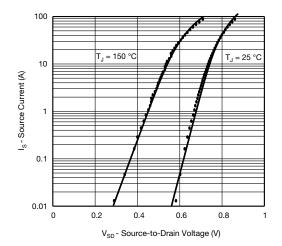












## Note

 Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.



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