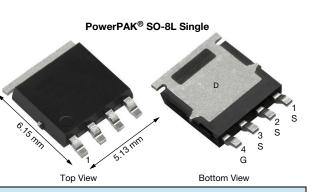
SiJA72ADP Vishay Siliconix

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PRODUCT SUMMARY	
V _{DS} (V)	40
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.00342
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.00478
Q _g typ. (nC)	14.8
I _D (A)	96
Configuration	Single

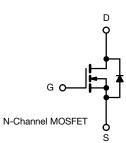
FEATURES

N-Channel 40 V (D-S) MOSFET

- TrenchFET[®] Gen IV power MOSFET
- Tuned for the lowest R_{DS}-Q_{oss} FOM
- 100 % R_q and UIS tested
- Q_{gd}/Q_{gs} ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- DC/AC inverters
- Battery and load switch



ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SiJA72ADP-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	40	V	
Gate-source voltage		V _{GS}	+20, -16	- V	
	T _C = 25 °C		96	_	
Continuous drain surrent (T 150 °C)	T _C = 70 °C		77		
Continuous drain current ($T_J = 150 \ ^{\circ}C$)	T _A = 25 °C	I _D	27.9 ^{b, c}		
	T _A = 70 °C		22.4 ^{b, c}		
Pulsed drain current (t = 100 µs)	•	I _{DM}	150	— A	
Continuous source-drain diode current	T _C = 25 °C		51.7		
	T _A = 25 °C	I _S	4.4 ^{b, c}		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	15		
Single pulse avalanche Energy	L = 0.1 MH	E _{AS}	11.25	mJ	
	T _C = 25 °C		56.8	w	
Manimum manual disain sting	T _C = 70 °C		36.4		
Maximum power dissipation	T _A = 25 °C	P _D	4.8 ^{b, c}		
	T _A = 70 °C	1	3.1 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	**	
Soldering recommendations (peak temperature) d, e			260		

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	t ≤ 10 s	R _{thJA}	22	26	°C/W
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.8	2.2	C/ W

Notes

a. T_C = 25 °C

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

f. Maximum under steady state conditions is 70 °C/W

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HALOGEN

FREE

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SiJA72ADP Vishay Siliconix

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			•	•			
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	40	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	/T		22	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-5.4	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1	-	2.4	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = +20, -16 V$	-	-	± 100	nA	
		$V_{DS} = 40 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	^	
Zero gate voltage drain current	IDSS	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$	-	-	10	μA	
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	30	-	-	А	
		V _{GS} = 10 V, I _D = 10 A -		0.00285	0.00342		
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	-	0.00398	0.00478	- Ω	
Forward transconductance ^a	g _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	-	76	-	S	
Dynamic ^b	·		•		1		
Input capacitance	C _{iss}		-	2530	-	pF	
Output capacitance	C _{oss}		-	465	-		
Reverse transfer capacitance		$V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz$	-	19	-		
C _{rss} /C _{iss} ratio			-	0.0075	0.0150		
	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	50					
Total gate charge			-	14.8	23	nC	
Gate-source charge	Q _{qs}	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 26 \text{ A}$	-	8.2	-		
Gate-drain charge	Q _{gd}		-	2.3	-		
Output charge	Q _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$	-	17.6	27		
Gate resistance	Rg	f = 1 MHz	0.26	1.3	2.6	Ω	
Turn-on delay time	t _{d(on)}		-	15	30		
Rise time	t _r	$V_{DD} = 20 \text{ V}, \text{ R}_{L} = 1 \Omega$	-	7	14		
Turn-off delay time	t _{d(off)}	$I_D \cong 20.8 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	35	70		
Fall time	t _f		-	5	10		
Turn-on delay time	t _{d(on)}		-	30	60	ns	
Rise time	t _r	$V_{DD} = 20 \text{ V}, \text{ R}_{L} = 1 \Omega$	-	150	300		
Turn-off delay time	t _{d(off)}	$I_D \cong 20.8$ Å, V_{GEN} = 4.5 V, R_g = 1 Ω	-	35	70		
Fall time	t _f		-	14	28		
Drain-Source Body Diode Characteristic	s			•			
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	51.7		
Pulse diode forward current ($t_p = 100 \ \mu s$)	I _{SM}		-	-	150	A	
Body diode voltage	V _{SD}	I _S = 10 A	-	0.74	1.1	V	
Body diode reverse recovery time	t _{rr}		-	22	44	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 20.8 A, di/dt = 100 A/μs,	-	10	20	nC	
Reverse recovery Fall time	t _a	$T_{\rm J} = 25 \ ^{\circ}{\rm C}$	-	12	-		
Reverse recovery rise time	t _b		-	10	-	ns	

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

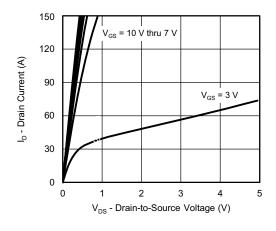
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

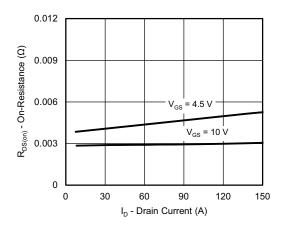
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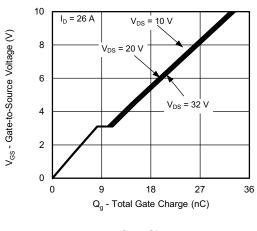
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



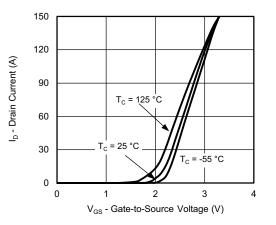
Output Characteristics



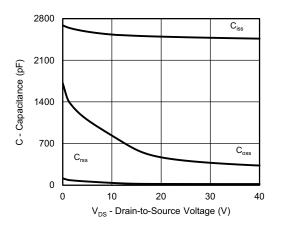
On-Resistance vs. Drain Current



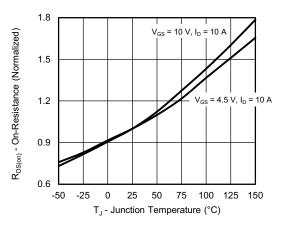
Gate Charge



Transfer Characteristics



Capacitance



On-Resistance vs. Junction Temperature

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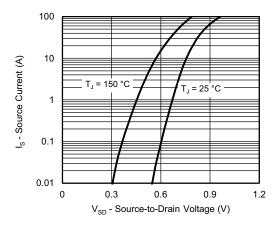
3

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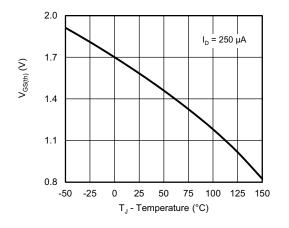
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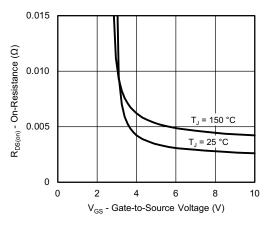
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



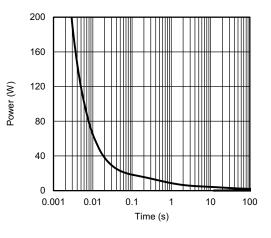
Source-Drain Diode Forward Voltage



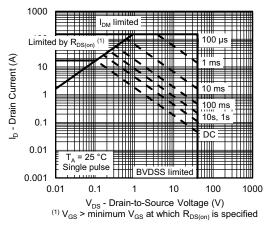
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



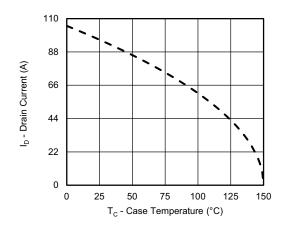
Safe Operating Area

4

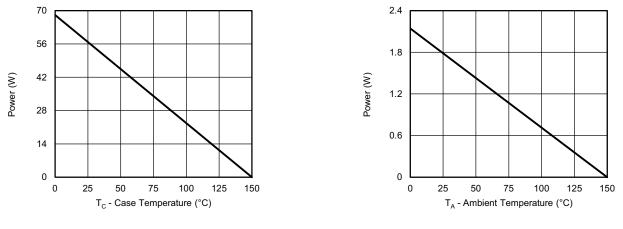
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



Power, Junction-to-Case

Power, Junction-to-Ambient

Note

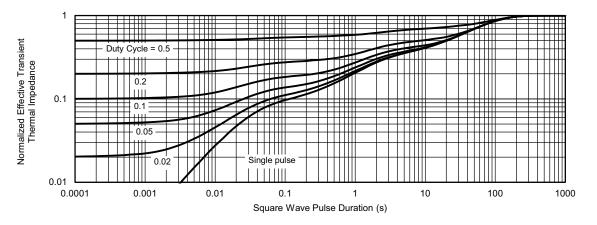
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



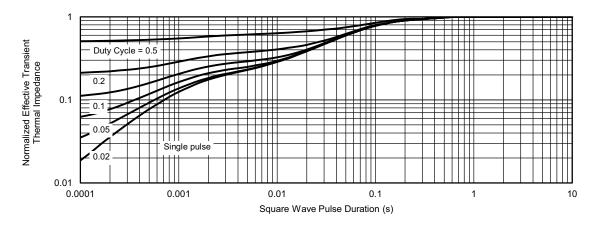
SiJA72ADP

Vishay Siliconix

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75342.

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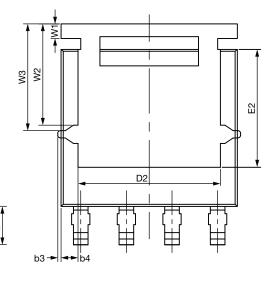


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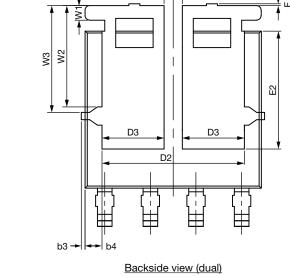
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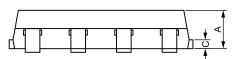




Topside view

Backside view (single)





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Package Information



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DIM	MILLIMETERS			INCHES				
DIM.	MIN.	NOM.	MAX.	MIN.	MIN. NOM.			
А	1.00	1.07	1.14	0.039	0.042	0.045		
A1	0.00	-	0.127	0.00	-	0.005		
b	0.33	0.41	0.48	0.013	0.016	0.019		
b1	0.44	0.51	0.58	0.017	0.020	0.023		
b2	4.80	4.90	5.00	0.189	0.193	0.197		
b3		0.094			0.004			
b4		0.47			0.019			
С	0.20	0.25	0.30	0.008	0.010	0.012		
D	5.00	5.13	5.25	0.197	0.202	0.207		
D1	4.80	4.90	5.00	0.189	0.193	0.197		
D2	3.86	3.96	4.06	0.152	0.156	0.160		
D3	1.63	1.73	1.83	0.064	0.068	0.072		
е		1.27 BSC		0.050 BSC				
E	6.05	6.15	6.25	0.238	0.242	0.246		
E1	4.27	4.37	4.47	0.168	0.172	0.176		
E2	3.18	3.28	3.38	0.125	0.129	0.133		
F	-	-	0.15	-	-	0.006		
L	0.62	0.72	0.82	0.024	0.028	0.032		
L1	0.92	1.07	1.22	0.036	0.042	0.048		
К		0.51			0.020			
W		0.23		0.009				
W1	0.41			0.016				
W2		2.82		0.111				
W3		2.96		0.117				
θ	0°	-	10°	0°	-	10°		

Note

• Millimeters will gover



RECOMMENDED MINIMUM PAD FOR PowerPAK[®] SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)

Revision: 07-Feb-12



Vishay

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