

N-Channel 100 V (D-S) MOSFET

DESCRIPTION

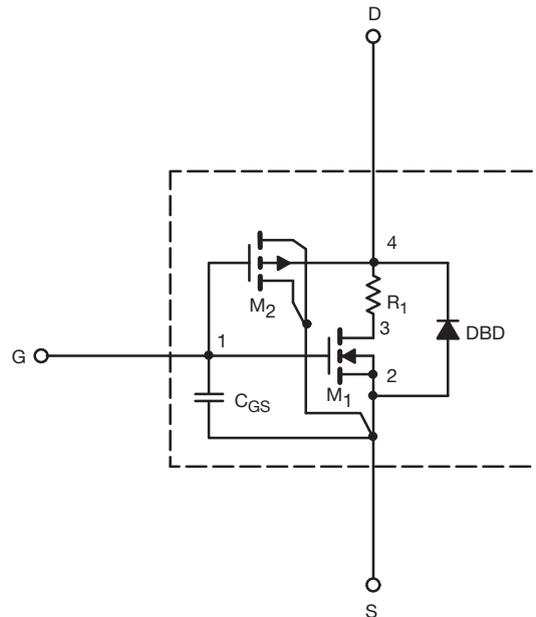
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



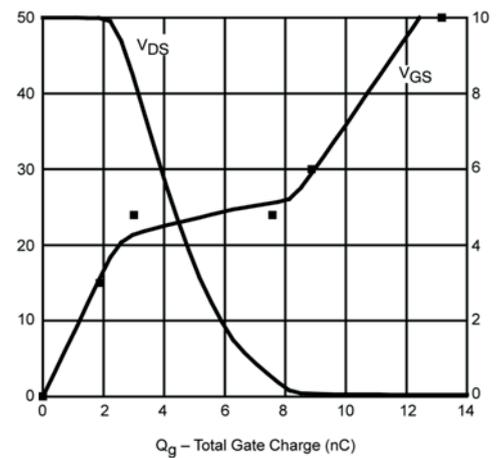
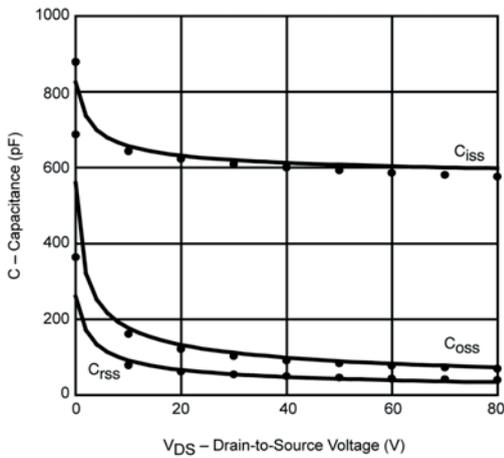
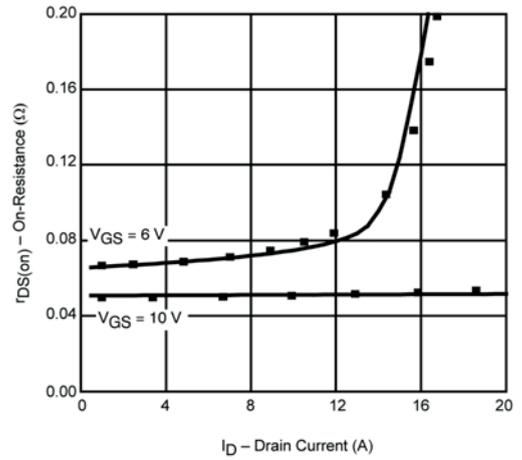
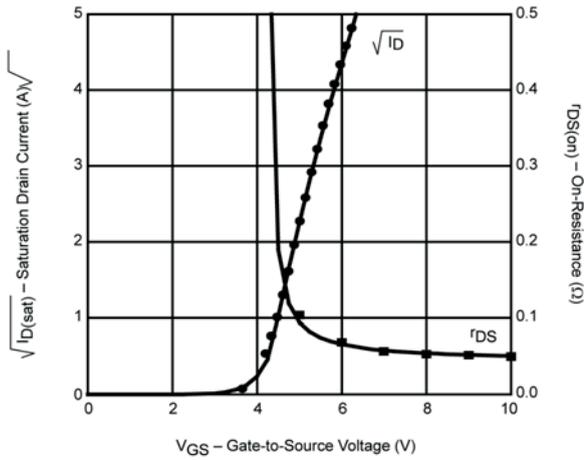
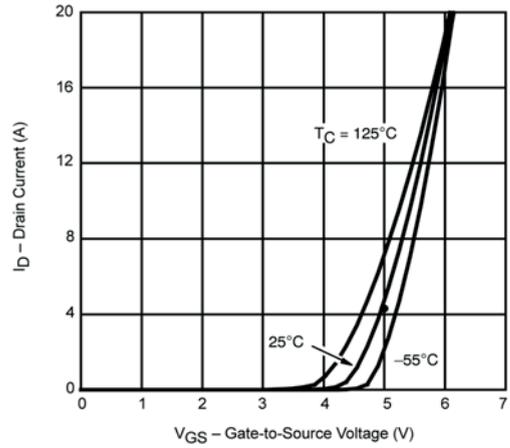
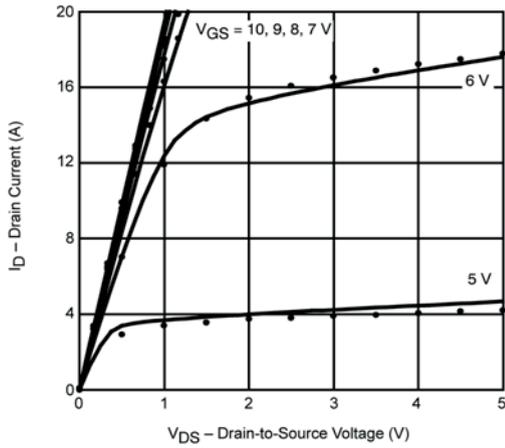
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	3	-	V
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	88	-	A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 5.4 A	0.051	0.052	Ω
		V _{GS} = 6 V, I _D = 4.6 A	0.069	0.070	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 5.4 A	12	12	S
Body Diode Voltage ^a	V _{SD}	I _S = 3.2 A, V _{GS} = 0 V	0.70	0.78	V
Dynamic^b					
Total Gate Charge	Q _g	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 5.4 A	13	13.5	nC
Gate-Source Charge	Q _{gs}		3	3	
Gate-Drain Charge	Q _{gd}		4.6	4.6	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 50 V, R _L = 50 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω	12	10	ns
Rise Time	t _r		16	15	
Turn-Off Delay Time	t _{d(off)}		20	20	
Fall Time	t _f		33	15	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data.