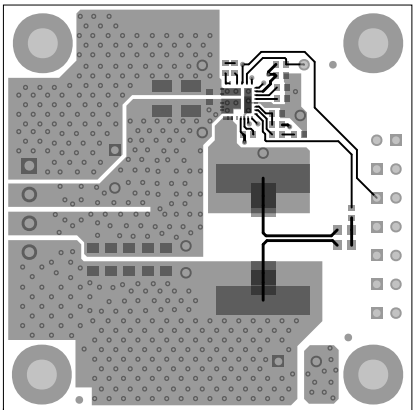
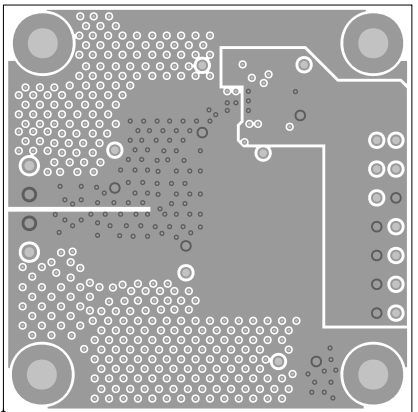
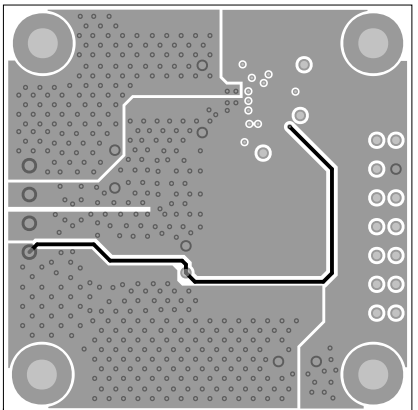


	LAYER: 01 PRIMARY-SIDE	COMPANY NAME: Vishay/Siliconix	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL ANGLE X ± .1 ± 5 XX ± .01 MACH FINISH XXX ± .005 ✓
	DESIGNER: TD	PROJECT NAME: SIC46X UNIFIED LOW POWER DEMO	
	CHECKER: INITIAL		
	DATE: 26AUG17	PROJECT NUMBER: NUMBER	REV. 2
	JOB#:		

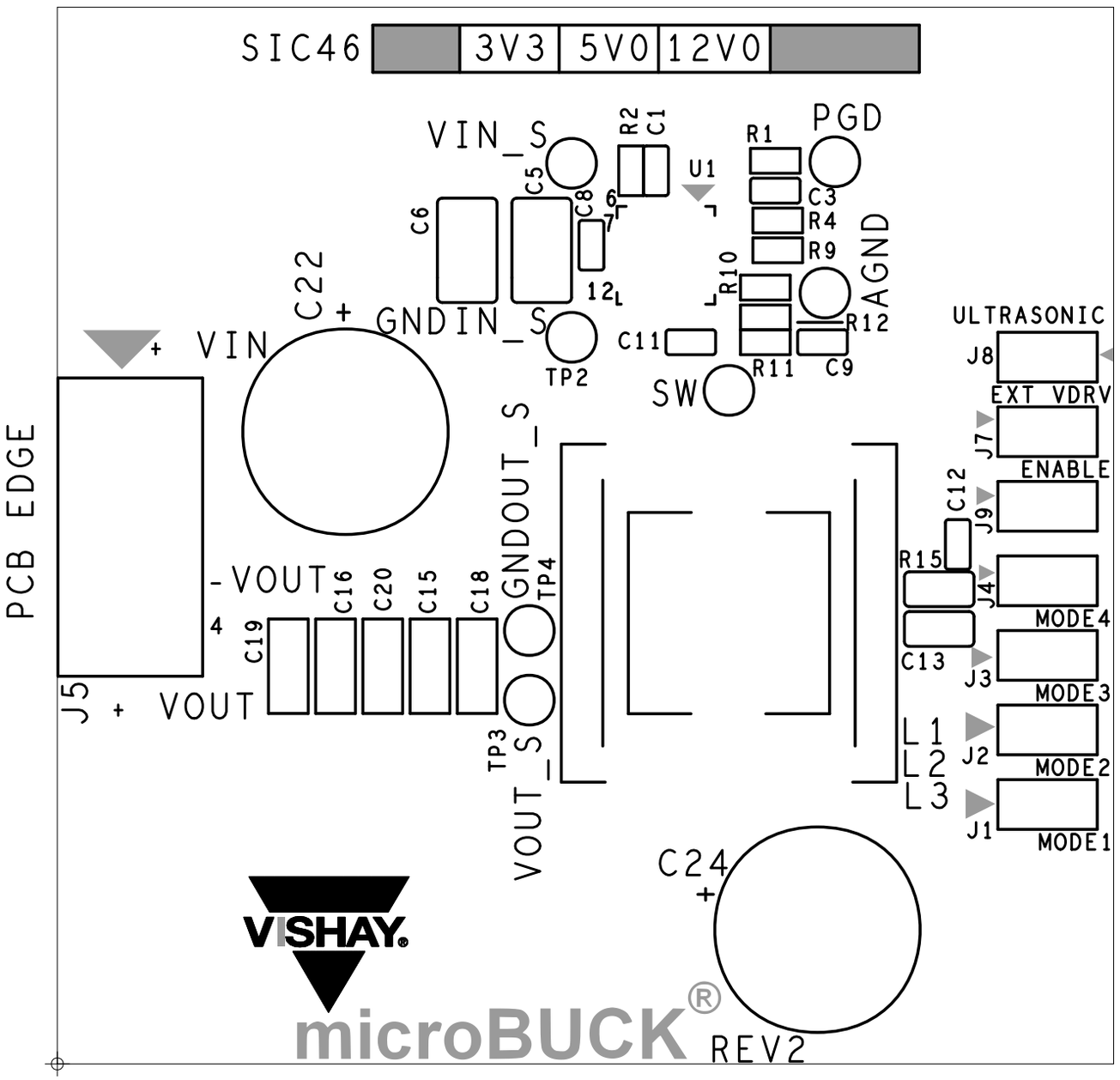


	INNER_LAYER2	COMPANY NAME: Vishay/Siliconix		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL ANGLE X ± .1 ± 5 XX ± .01 MACH FINISH XXX ± .005 ✓
	DESIGNER: TD	PROJECT NAME: SIC46X UNIFIED LOW POWER DEMO		
	CHECKER: INITIAL			
	DATE: 26AUG17	PROJECT NUMBER: NUMBER	REV. 2	
	JOB#:			

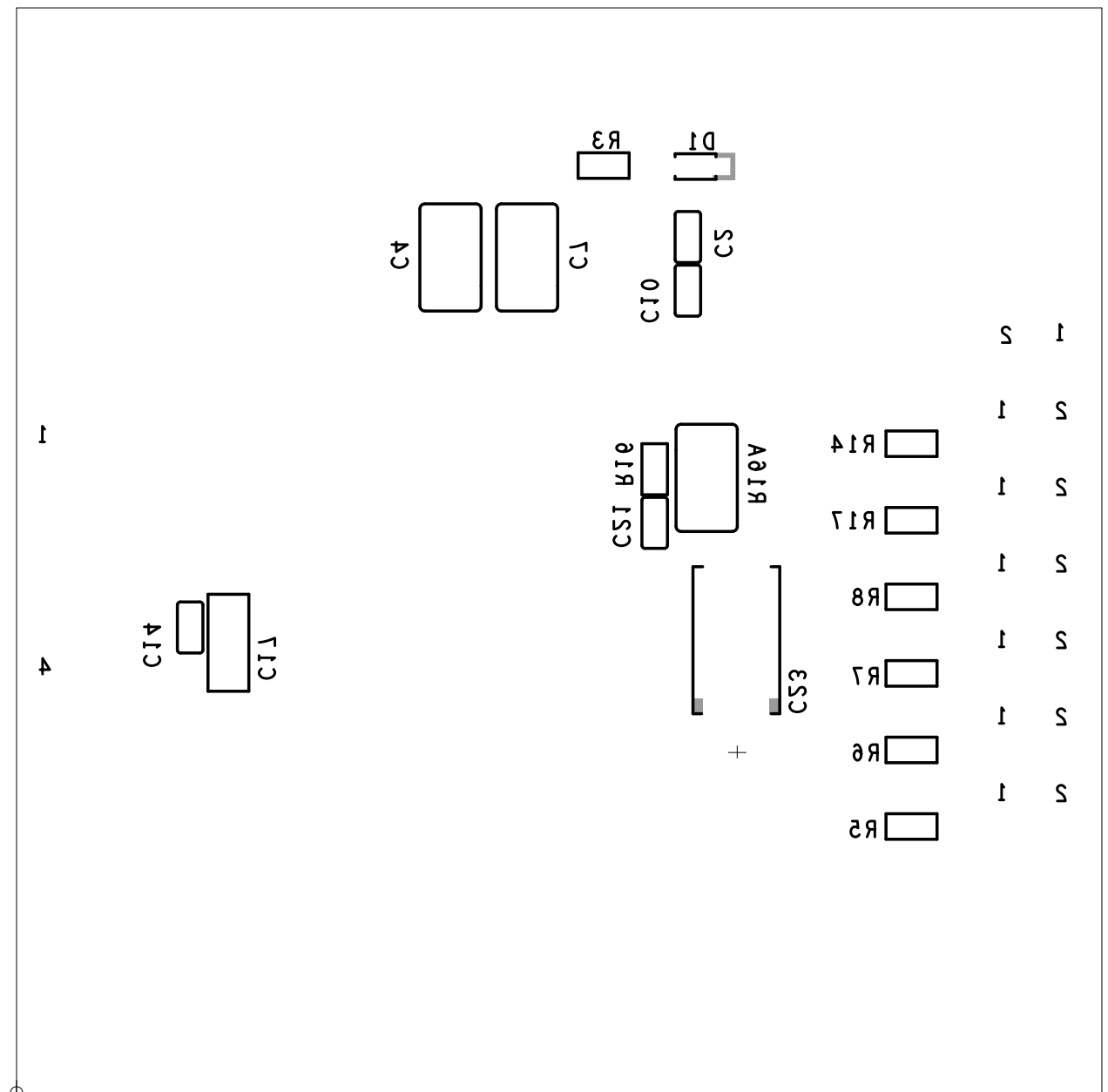


	INNER_LAYER3	COMPANY NAME: Vishay/Siliconix		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL ANGLE X ± .1 ± 5 XX ± .01 MACH FINISH XXX ± .005 ✓
	DESIGNER: TD	PROJECT NAME: SIC46X UNIFIED LOW POWER DEMO		
	CHECKER: INITIAL			
	DATE: 26AUG17	PROJECT NUMBER: NUMBER	REV. 2	
	JOB#:			

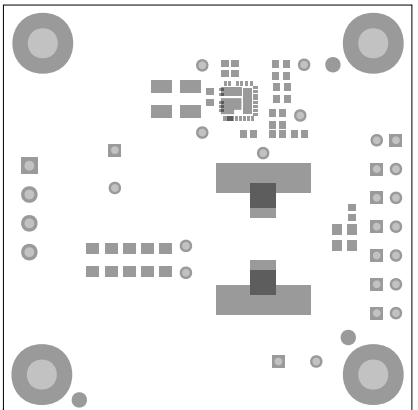
	LAYER:04 SECONDARY-SIDE	COMPANY NAME: Vishay/Siliconix	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER: TD	PROJECT NAME: SIC46X UNIFIED LOW POWER DEMO	
	CHECKER: INITIAL		TOLERANCES DECIMAL ANGLE X ±.1 ± 5 XX ±.01 MACH FINISH XXX ±.005 √
	DATE: 26AUG17	PROJECT NUMBER: NUMBER	REV. 2
	JOB#:		


SIC46
3V3
5V0
12V0
VIN_S
R2
C1
U1
R1
PGD
C5
C8
C6
C3
R4
R9
R10
AGND
C22
VIN
GNDIN_S
TP2
C11
R12
R11
C9
SW
ULTRASONIC
J8
EXT VDRV
J7
ENABLE
J9
C12
PCB EDGE
-VOUT
C16
C20
C15
C18
GNDOUT_S
TP4
R15
J4
MODE4
C19
C13
J3
MODE3
J5
VOUT
TP3
VOUT_S
L1
L2
L3
J2
MODE2
J1
MODE1
C24
VISHAY
microBUCK®
REV2

SILKTOP

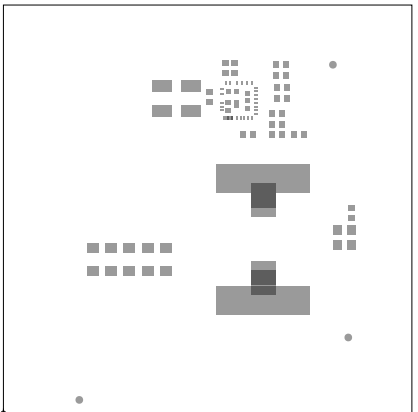


SILK BOTTOM



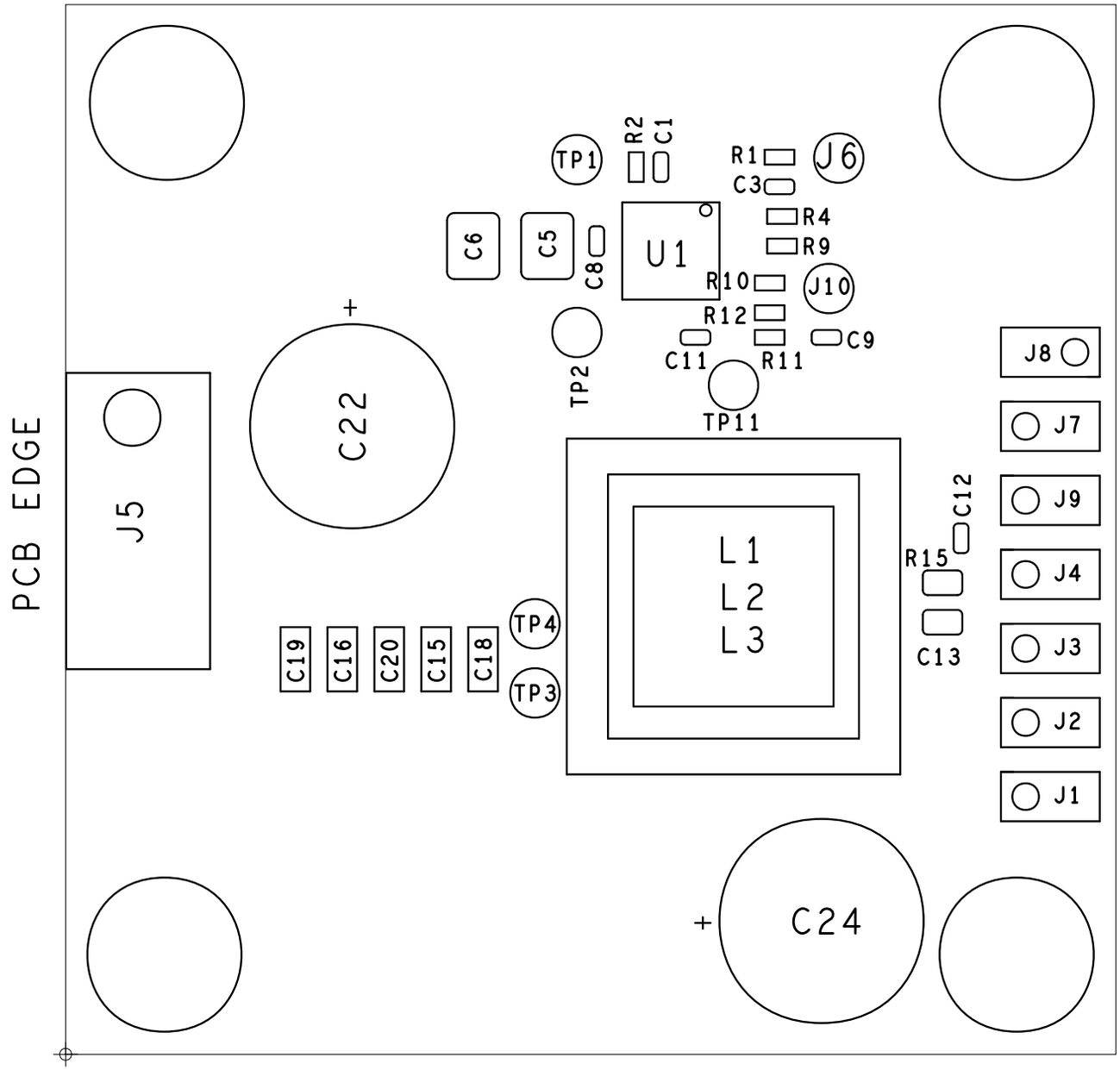
	SOLDERMASK PRIMARY-SIDE	COMPANY NAME: Vishay/Siliconix	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL X ± .1 XX ± .01 XXX ± .005 ANGLE ± 5 MACH FINISH ✓
	DESIGNER: TD	PROJECT NAME: SIC46X UNIFIED LOW POWER DEMO	
	CHECKER: INITIAL		
	DATE: 26AUG17	PROJECT NUMBER: NUMBER	REV. 2
	JOB#:		

	SOLDERMASK SECONDARY-SIDE	COMPANY NAME: Vishay/Siliconix	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER: TD	PROJECT NAME: SIC46X UNIFIED LOW POWER DEMO	
	CHECKER: INITIAL		TOLERANCES DECIMAL ANGLE X ±.1 ± 5 XX ±.01 MACH FINISH XXX ±.005 √
	DATE: 26AUG17	PROJECT NUMBER: NUMBER	REV. 2
	JOB#:		

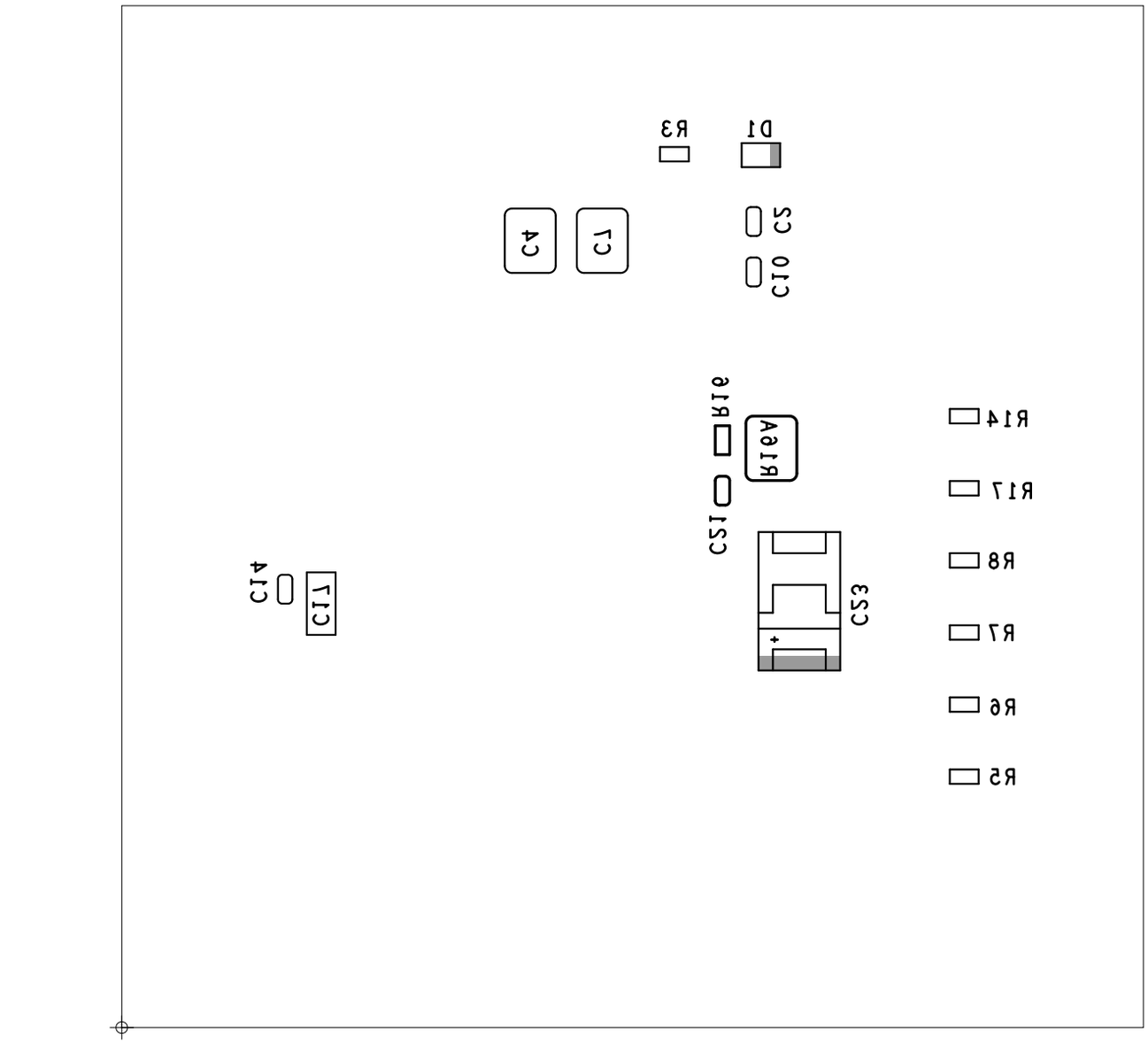


	PASTEMASK PRIMARY-SIDE	COMPANY NAME: Vishay/Siliconix	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL ANGLE X ± .1 ± 5 XX ± .01 MACH FINISH XXX ± .005 ✓
	DESIGNER: TD	PROJECT NAME: SIC46X UNIFIED LOW POWER DEMO	
	CHECKER: INITIAL		
	DATE: 26AUG17	PROJECT NUMBER: NUMBER	REV. 2
	JOB#:		

	PASTEMASK SECONDARY-SIDE	COMPANY NAME: Vishay/Siliconix	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
	DESIGNER: TD	PROJECT NAME: SIC46X UNIFIED LOW POWER DEMO	
	CHECKER: INITIAL		TOLERANCES DECIMAL ANGLE X ±.1 ± 5 XX ±.01 MACH FINISH XXX ±.005 √
	DATE: 26AUG17	PROJECT NUMBER: NUMBER	REV. 2
	JOB#:		

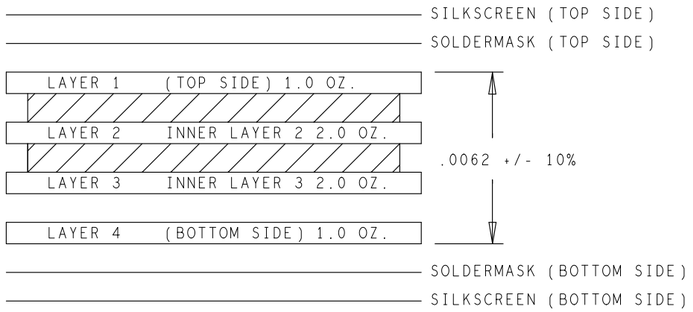


ASSEMBLY TOP



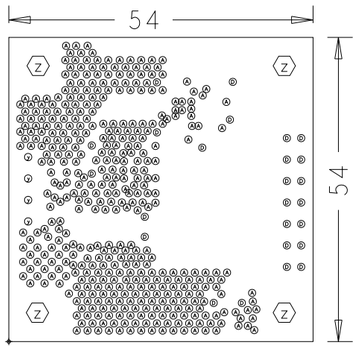
ASSEMBLY BOTTOM

LAYER DETAIL
4 LAYER



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
⊗	13.0	+3.0/-13.0	PLATED	418
⊛	40.0	+3.0/-3.0	PLATED	25
⊙	51.0	+3.0/-3.0	PLATED	4
ⓩ	156.0	+3.0/-3.0	PLATED	4



FAB NOTE

FAB NOTES: UNLESS OTHERWISE SPECIFIED.

1. PART NUMBER — P/N 133-020-0002
2. SIDE SHOWN — PRIMARY / SIDE 1.
3. DIMENSIONS — DECIMAL INCHES.
4. BASE MATERIAL — LEAD-FREE PROCESS
5. Tg — MINIMUM GLASS TRANSITTION TEMPERATURE (Tg) OF 170 DEGREES CELSIUS.
6. FLAME CLASS — UL 94V-0 & MUST MEET REQUIREMENTS OF UL 796.
7. MOT — MANUFACTURE MUST BE UL RECOGNIZED TO PRODUCE THIS PRODUCT SUCH THAT IT MEETS 130 DEGREES CELSIUS MAXIMUM OPERATING TEMPERATURE (MOT).
8. MARKINGS — THE FOLLOWING MUST BE MARKED OR ETCHED ON SIDE 2 OF PCB IN AREA SHOWN:
   DATE CODE.
   UL RECOGNIZED VENDOR ID UL TYPE DESIGNATION AND/OR MARKINGS WHICH REPLECT THE SPECIFIED FLAME CLASS AND MAXIMUM OPERATING TEMPERATURE RATTINGS.
9. PCB THICKNESS — 0.62 +/-10% AS MESURED OVER METAL.
10. BOW & TWIST — SHALL BE DETERMINED BY PHYSICAL MEASUREMENT AND PERCENTAGE CALCULATION IN ACCORDANCE WITH IPC - TM - 650. METHOD 2.4.22.
11. PLATING — MINIMUM COPPER THICKNESS AFTER PROCESSING INTERNAL AND EXTERNAL LAYERS IS PROVIDED BELOW IN THE LAYER STACKUP.
    HOLE PLATING = 0.001 MIN. AVERAGE / 0.0008 ABSOLUTE MIN PLATING.
    HOLE DIAMETERS SPECIFIED AFTER PLATING (SEE HOLE SCHEDULE).
12. CONDUCTORS — FINISHED CONDUCTOR WIDTH: 0.010 REDUCED NO MORE THAN 20% OF NOMINAL.
    FINISHED CONDUCTOR SPACING: 0.003 MINIMUM.
13. ANNULAR RING — 0.001 MINIMUM FOR INTERNAL ANNULAR RING.
    0.002 MINIMUM FOR EXTERNAL ANNULAR RING.
14. Minimum immersion gold thickness of 2uin - 8uin over a minimum of 118uin electroless nickel.
15. When applies Gold Plating and Nickel Plating For Edge-Board Connectors and Non-Soldered Areas Shall be Per IPC-2221
    Unless Otherwise Specified on the Fabrication Drawing.
    For none functional short gold fingers it is ok to leave the plating trace
16. SOLDER MASK — TO BE IN ACCORDANCE WITH IPC-SM-840C CLASS T.
    TYPE: LIQUID PHOTOIMAGEABLE.
    BRAND: CIBA-GEIGY PROBIMER 52, 65M, ENTHONE ENPLATE DSR-3241 OR EQUIVALENT.
    FINISH: MATTE FINISH PREFERRED.
    COLOR: LIGHT BLUE (OR CLOSEST)
    REGISTRATION: TO BE WITHIN +/-0.003 OF ITS RESPECTIVE OUTER CIRCUIT LAYERS.
    SOLDER MASK ENCROACHMENT ONTO SMT LANDS IS INTENTIONAL
    WHERE SUPPLIED DATA DOES NOT PROVIDE CLEARANCE FROM THE PAD.
17. SOLDER MASK COLOR: LIGHT BLUE (OR CLOSEST)
18. FINISH — SOLDER MASK OVER BARE COPPER (SMOBC) WITH HOT AIR SOLDER LAVELING (HASL).
19. SILKSCREEN — WHITE NONCONDUCTIVE INK.
    NO INK TO APPEAR ON EXPOSED COPPER SUCH AS PLATE THROUGH HOLE PADS AND SURFACE MOUNT LANDS. INK ON SOLDER MASK COVERED PADS IS PERMISSIBLE.
20. LAYER STACKUP — 4 LAYERS. SEE STACK-UP DETAIL.
21. TOTAL THICKNESS — 0.062".
22. FIDUCIALS — ADD FIDUCIALS TO PRIMARY SIDES.
23 MATERIAL: — LEAD-FREE PROCESS
24 COLOR: — LIGHT BLUE (OR CLOSEST)
25 COPPER THICKNESS: — SEE STACK-UP DETAIL.

	FAB DRAWING	COMPANY NAME: Vishay/Siliconix		UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES DECIMAL ANGLE X±.1 ±5 XX±.01 MACH FINISH XXX±.005 ✓
	DESIGNER: TD CHECKER: INITIAL DATE: 26AUG17 JOB#:	PROJECT NAME: SIC46X_UNIFIED_LOW_POWER_DEMO		
		FAB NUMBER: NUMBER	REV. 2	SHEET: 1 OF 2