

Vishay Siliconix

# Automotive P-Channel 40 V (D-S) 175 °C MOSFET

### DESCRIPTION

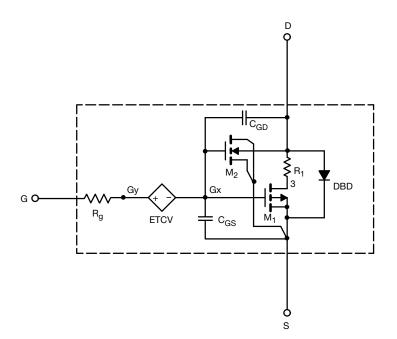
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## CHARACTERISTICS

- P-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

## SUBCIRCUIT MODEL SCHEMATIC



#### Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



SPICE Device Model SQJ423EP

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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \ \mu A$	2	-	V
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = -10 \text{ V}, I_D = -10 \text{ A}$	0.011	0.011	Ω
		$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -5 \text{ A}$	0.018	0.018	
Forward transconductance <sup>a</sup>	<b>g</b> <sub>fs</sub>	$V_{DS} = -15 \text{ V}, \text{ I}_{D} = -10 \text{ A}$	30	29	S
Diode forward voltage	V <sub>SD</sub>	I <sub>S</sub> = -10 A	-0.8	-0.8	V
Dynamic <sup>b</sup>					
Input capacitance	C <sub>iss</sub>	$V_{DS}$ = -25 V, $V_{GS}$ = 0 V, f = 1 MHz	3670	3300	pF
Output capacitance	C <sub>oss</sub>		435	435	
Reverse transfer capacitance	C <sub>rss</sub>		336	335	
Total gate charge	Qg	V <sub>DS</sub> = -20 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -5 A	73	80	nC
Gate-source charge	Q <sub>gs</sub>		10	10	
Gate-drain charge	Q <sub>gd</sub>		22	22	

Notes

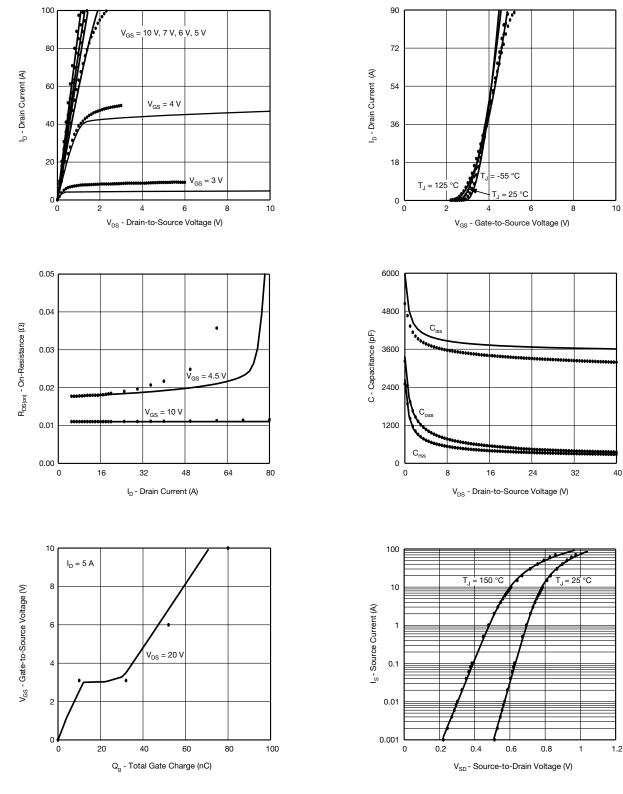
a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$ 

b. Guaranteed by design, not subject to production testing



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## COMPARISON OF MODEL WITH MEASURED DATA (T\_J = 25 °C, unless otherwise noted)



### Note

Dots and squares represent measured data
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