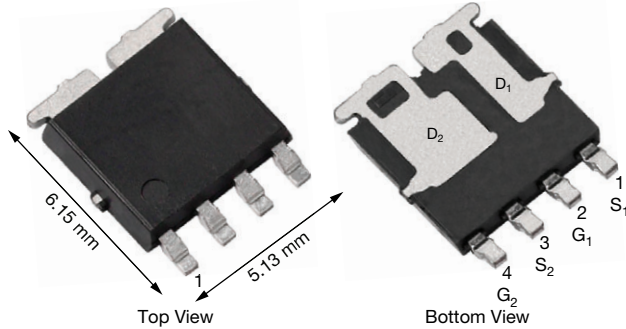


Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFETs

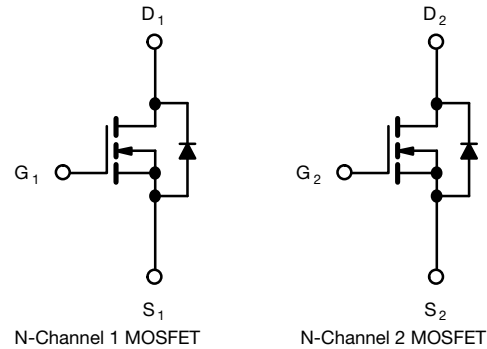
PowerPAK® SO-8L Dual Asymmetric

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Optimized for synchronous buck applications
- Material categorization:
for definitions of compliance please see www.vishay.com/doc?99912

 AUTOMOTIVE
GRADE

RoHS
COMPLIANT
HALOGEN
FREE

| PRODUCT SUMMARY | | |
|--|---------------------------|-------------|
| | N-CHANNEL 1 | N-CHANNEL 2 |
| V _{DS} (V) | 40 | 40 |
| R _{DS(on)} (Ω) at V _{GS} = 10 V | 0.0110 | 0.0045 |
| R _{DS(on)} (Ω) at V _{GS} = 4.5 V | 0.0150 | 0.0060 |
| I _D (A) | 20 | 60 |
| Configuration | Dual | |
| Package | PowerPAK SO-8L asymmetric | |



| ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted) | | | | |
|---|-----------------------------------|-------------------------|-----------------|------|
| PARAMETER | SYMBOL | N-CHANNEL 1 | N-CHANNEL 2 | UNIT |
| Drain-source voltage | V _{DS} | 40 | 40 | V |
| Gate-source voltage | V _{GS} | ± 20 | | |
| Continuous drain current | I _D | T _C = 25 °C | 20 ^a | A |
| | | T _C = 125 °C | 20 ^a | |
| Continuous source current (diode conduction) | I _S | 20 ^a | 44 | A |
| Pulsed drain current ^b | I _{DM} | 80 | 170 | |
| Single pulse avalanche current | I _{AS} | L = 0.1 mH | 19 | mJ |
| Single pulse avalanche energy | | | E _{AS} | |
| Maximum power dissipation ^b | P _D | T _C = 25 °C | 27 | W |
| | | T _C = 125 °C | 9 | |
| Operating junction and storage temperature range | T _J , T _{stg} | -55 to +175 | | °C |
| Soldering recommendations (peak temperature) ^{d, e} | | 260 | | |

| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------|-------------------|-------------|-------------|------|
| PARAMETER | SYMBOL | N-CHANNEL 1 | N-CHANNEL 2 | UNIT |
| Junction-to-ambient | R _{thJA} | 85 | 85 | °C/W |
| Junction-to-case (drain) | | | | |

Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



| SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|--|--------------|---|---|--------|------|---------|-----------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | N-Ch 1 | 40 | - | - |
| | | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | N-Ch 2 | 40 | - | - |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | N-Ch 1 | 1.5 | 2.0 | 2.5 |
| | | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | N-Ch 2 | 1.5 | 2.0 | 2.5 |
| Gate-source leakage | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | N-Ch 1 | - | - | ± 100 |
| | | | | N-Ch 2 | - | - | ± 100 |
| Zero gate voltage drain current | I_{DSS} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}$ | N-Ch 1 | - | - | 1 |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}$ | N-Ch 2 | - | - | 1 |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | N-Ch 1 | - | - | 50 |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | N-Ch 2 | - | - | 50 |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$ | N-Ch 1 | - | - | 250 |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 40\text{ V}, T_J = 175\text{ }^\circ\text{C}$ | N-Ch 2 | - | - | 250 |
| On-state drain current ^a | $I_{D(on)}$ | $V_{GS} = 10\text{ V}$ | $V_{DS} \geq 5\text{ V}$ | N-Ch 1 | 15 | - | - |
| | | $V_{GS} = 10\text{ V}$ | $V_{DS} \geq 5\text{ V}$ | N-Ch 2 | 30 | - | - |
| Drain-source on-state resistance ^a | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 4\text{ A}$ | N-Ch 1 | - | 0.00890 | 0.01100 |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 10\text{ A}$ | N-Ch 2 | - | 0.00365 | 0.00450 |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 4\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | N-Ch 1 | - | - | 0.01600 |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 10\text{ A}, T_J = 125\text{ }^\circ\text{C}$ | N-Ch 2 | - | - | 0.00640 |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 4\text{ A}, T_J = 175\text{ }^\circ\text{C}$ | N-Ch 1 | - | - | 0.01890 |
| | | $V_{GS} = 10\text{ V}$ | $I_D = 10\text{ A}, T_J = 175\text{ }^\circ\text{C}$ | N-Ch 2 | - | - | 0.00740 |
| | | $V_{GS} = 4.5\text{ V}$ | $I_D = 3\text{ A}$ | N-Ch 1 | - | 0.01210 | 0.01500 |
| | | $V_{GS} = 4.5\text{ V}$ | $I_D = 8\text{ A}$ | N-Ch 2 | - | 0.00490 | 0.00600 |
| Forward transconductance ^b | g_{fs} | $V_{DS} = 10\text{ V}, I_D = 4\text{ A}$ | | N-Ch 1 | - | 26 | - |
| | | $V_{DS} = 10\text{ V}, I_D = 10\text{ A}$ | | N-Ch 2 | - | 73 | - |
| Dynamic ^b | | | | | | | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ | N-Ch 1 | - | 840 | 1200 |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ | N-Ch 2 | - | 2032 | 2800 |
| Output capacitance | C_{oss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ | N-Ch 1 | - | 662 | 900 |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ | N-Ch 2 | - | 1256 | 1700 |
| Reverse transfer capacitance | C_{rss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ | N-Ch 1 | - | 29 | 40 |
| | | $V_{GS} = 0\text{ V}$ | $V_{DS} = 25\text{ V}, f = 1\text{ MHz}$ | N-Ch 2 | - | 52 | 75 |
| Total gate charge ^c | Q_g | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 2\text{ A}$ | N-Ch 1 | - | 13 | 20 |
| | | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 4\text{ A}$ | N-Ch 2 | - | 28.5 | 45 |
| Gate-source charge ^c | Q_{gs} | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 2\text{ A}$ | N-Ch 1 | - | 2.4 | - |
| | | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 4\text{ A}$ | N-Ch 2 | - | 5.2 | - |
| Gate-drain charge ^c | Q_{gd} | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 2\text{ A}$ | N-Ch 1 | - | 1.5 | - |
| | | $V_{GS} = 10\text{ V}$ | $V_{DS} = 20\text{ V}, I_D = 4\text{ A}$ | N-Ch 2 | - | 3.3 | - |
| Gate resistance | R_g | $f = 1\text{ MHz}$ | | N-Ch 1 | 0.55 | 1.16 | 1.8 |
| | | | | N-Ch 2 | 0.25 | 0.54 | 0.85 |



| SPECIFICATIONS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|--|---------------|---|--------|------|------|------|----|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
| Dynamic ^b | | | | | | | |
| Turn-on delay time ^c | $t_{d(on)}$ | $V_{DD} = 20\text{ V}$, $R_L = 10\ \Omega$, $I_D \cong 2\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$ | N-Ch 1 | - | 10 | 15 | ns |
| | | $V_{DD} = 20\text{ V}$, $R_L = 5\ \Omega$, $I_D \cong 4\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$ | N-Ch 2 | - | 15 | 25 | |
| Rise time ^c | t_r | $V_{DD} = 20\text{ V}$, $R_L = 10\ \Omega$, $I_D \cong 2\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$ | N-Ch 1 | - | 4 | 10 | |
| | | $V_{DD} = 20\text{ V}$, $R_L = 5\ \Omega$, $I_D \cong 4\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$ | N-Ch 2 | - | 4 | 10 | |
| Turn-off delay time ^c | $t_{d(off)}$ | $V_{DD} = 20\text{ V}$, $R_L = 10\ \Omega$, $I_D \cong 2\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$ | N-Ch 1 | - | 19 | 30 | |
| | | $V_{DD} = 20\text{ V}$, $R_L = 5\ \Omega$, $I_D \cong 4\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$ | N-Ch 2 | - | 26 | 40 | |
| Fall time ^c | t_f | $V_{DD} = 20\text{ V}$, $R_L = 10\ \Omega$, $I_D \cong 2\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$ | N-Ch 1 | - | 9 | 15 | |
| | | $V_{DD} = 20\text{ V}$, $R_L = 5\ \Omega$, $I_D \cong 4\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\ \Omega$ | N-Ch 2 | - | 9 | 15 | |
| Source-Drain Diode Ratings and Characteristics ^b | | | | | | | |
| Pulsed current ^a | I_{SM} | | N-Ch 1 | - | - | 80 | A |
| | | | N-Ch 2 | - | - | 170 | |
| Forward voltage | V_{SD} | $I_F = 4\text{ A}$, $V_{GS} = 0\text{ V}$ | N-Ch 1 | - | 0.78 | 1.2 | V |
| | | $I_F = 10\text{ A}$, $V_{GS} = 0\text{ V}$ | N-Ch 2 | - | 0.78 | 1.2 | |
| Body diode reverse recovery time | t_{rr} | $I_F = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 1 | - | 38 | 80 | ns |
| | | $I_F = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 2 | - | 54 | 110 | |
| Body diode reverse recovery charge | Q_{rr} | $I_F = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 1 | - | 23 | 50 | nC |
| | | $I_F = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 2 | - | 61 | 125 | |
| Reverse recovery fall time | t_a | $I_F = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 1 | - | 13 | - | ns |
| | | $I_F = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 2 | - | 29 | - | |
| Reverse recovery rise time | t_b | $I_F = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 1 | - | 25 | - | |
| | | $I_F = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 2 | - | 25 | - | |
| Body diode peak reverse recovery current | $I_{RM(REC)}$ | $I_F = 4\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 1 | - | -1 | - | A |
| | | $I_F = 5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | N-Ch 2 | - | -1.8 | - | |

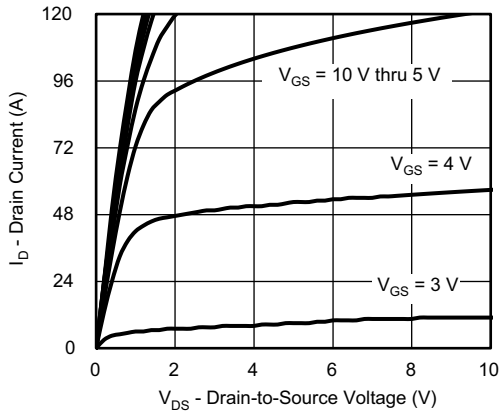
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

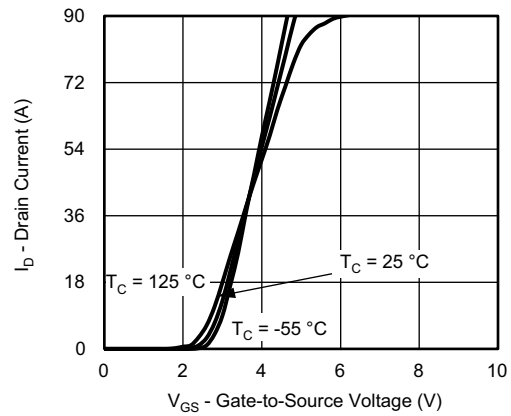
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



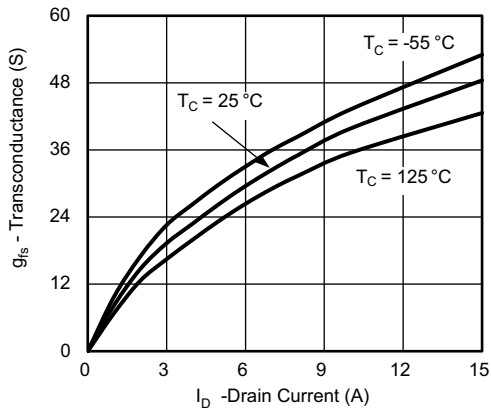
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



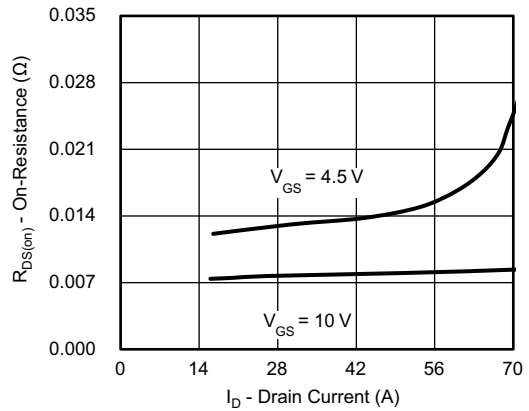
Output Characteristics



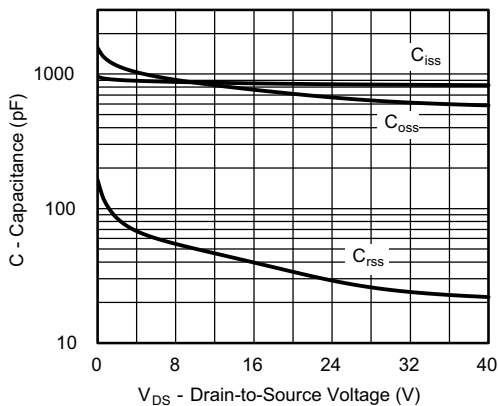
Transfer Characteristics



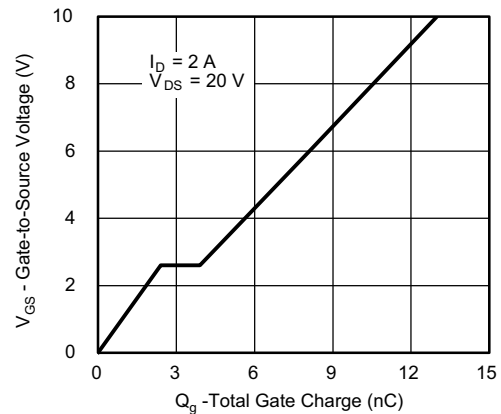
Transconductance



On-Resistance vs. Drain Current



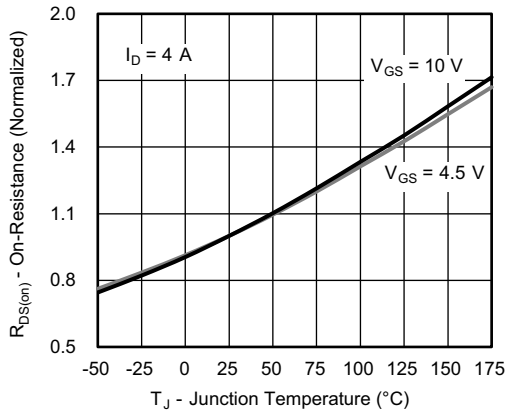
Capacitance



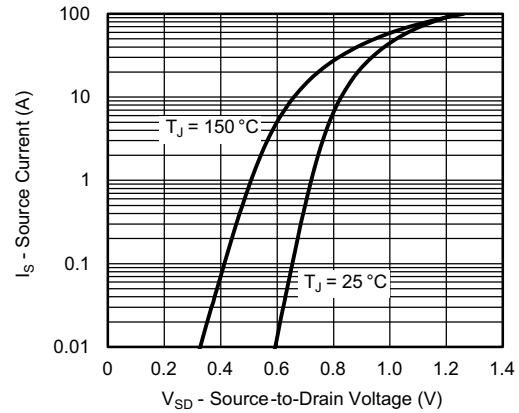
Gate Charge



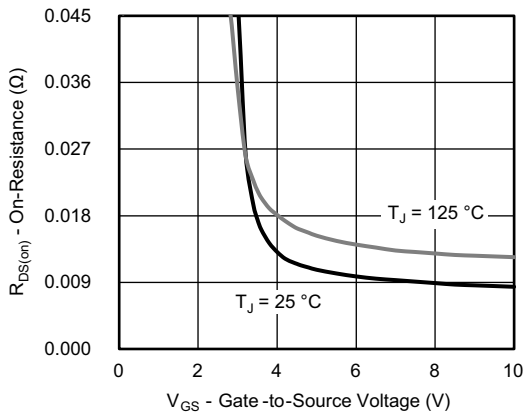
N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



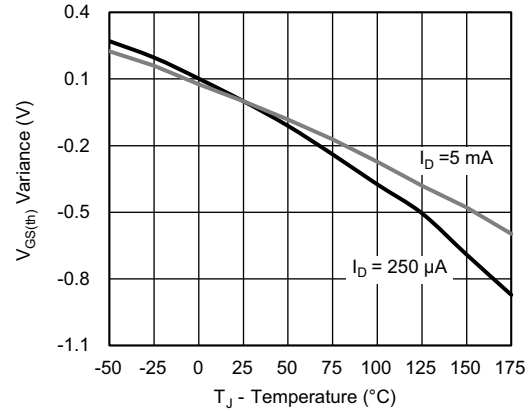
On-Resistance vs. Junction Temperature



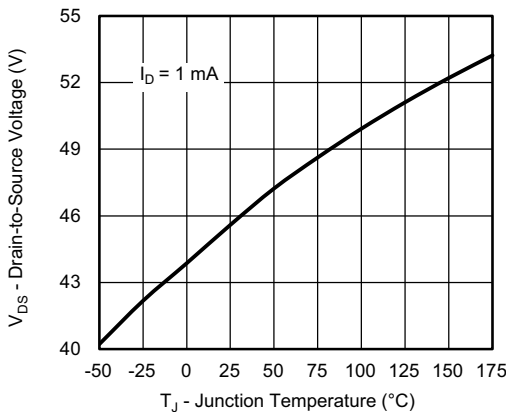
Source Drain Diode Forward Voltage



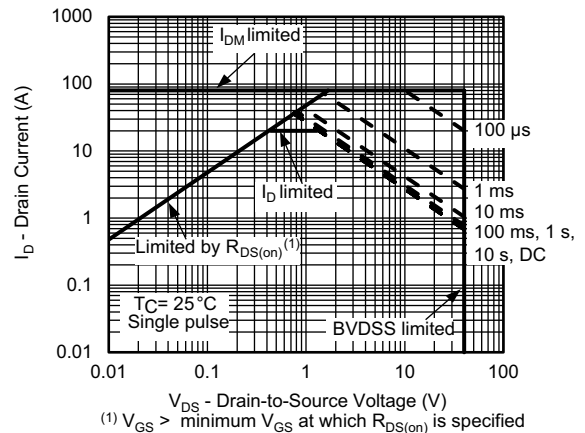
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



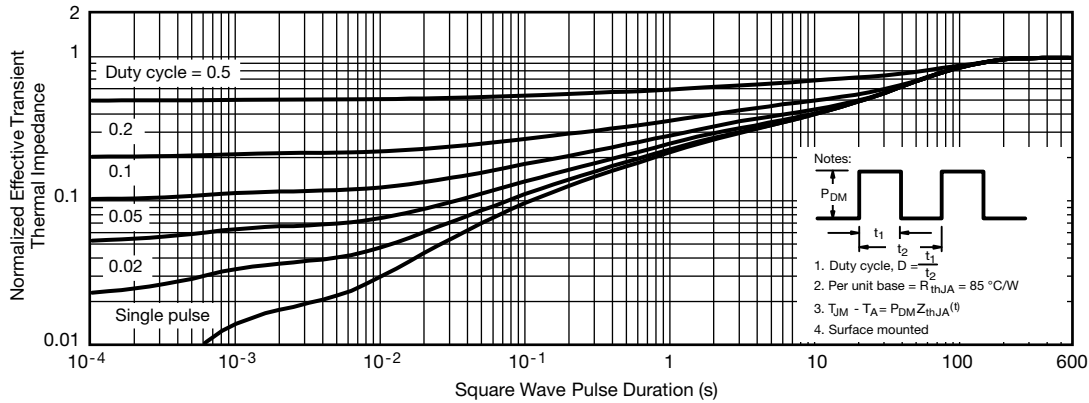
Drain Source Breakdown vs. Junction Temperature



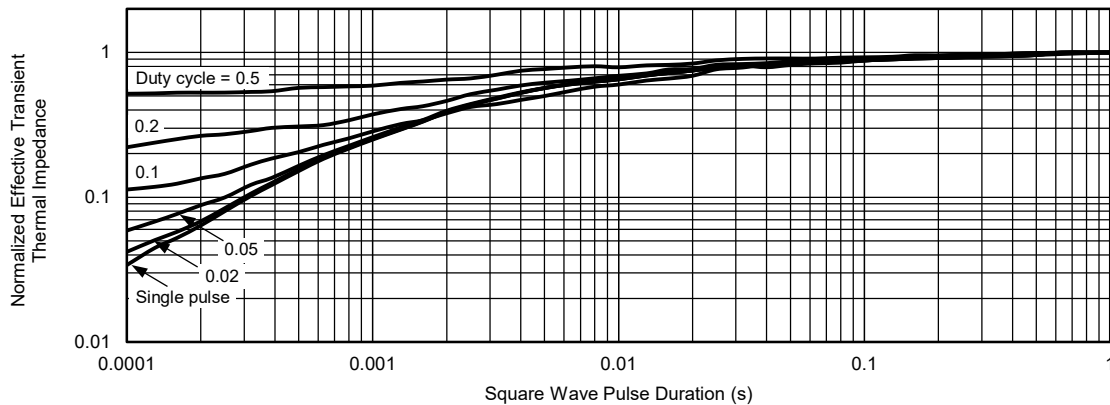
Safe Operating Area



N-CHANNEL 1 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

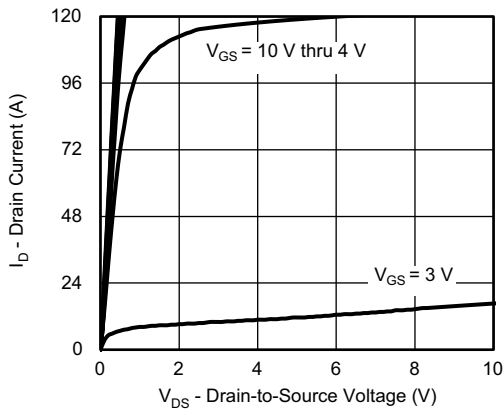


Normalized Thermal Transient Impedance, Junction-to-Case

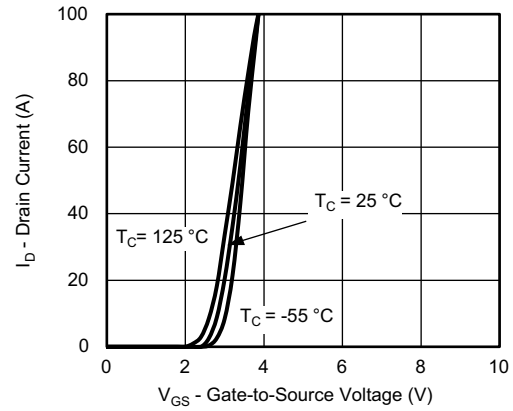
Note

- The characteristics shown in the graph:
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$) is given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

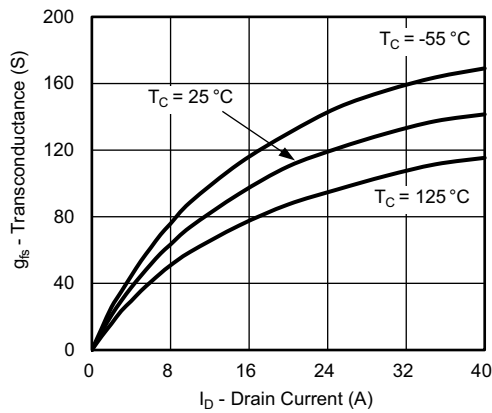
N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



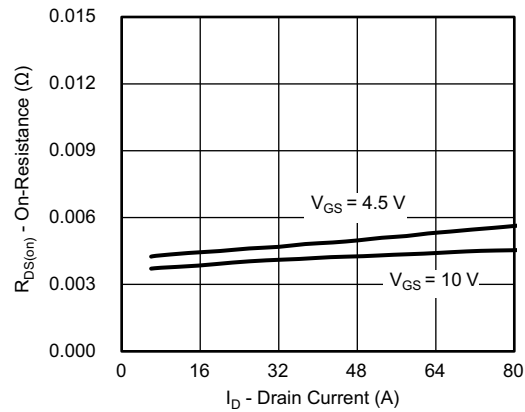
Output Characteristics



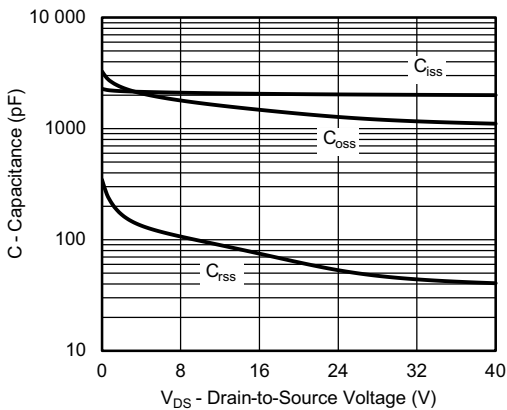
Transfer Characteristics



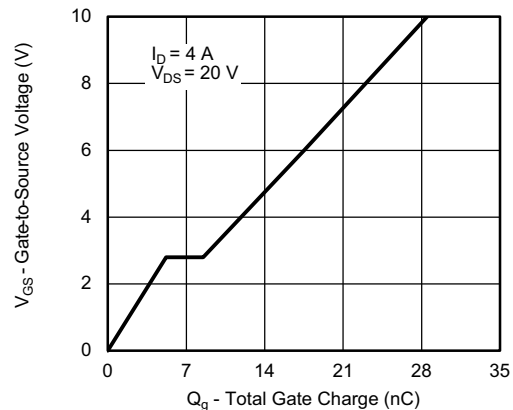
Transconductance



On-Resistance vs. Drain Current

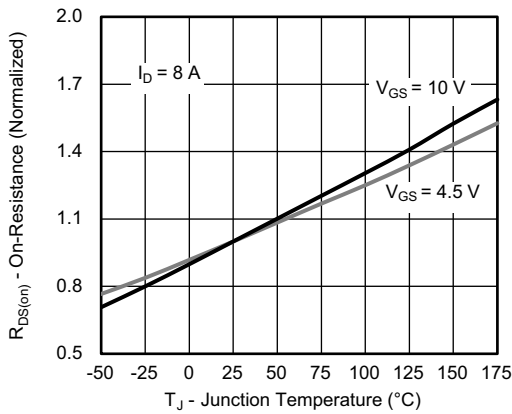


Capacitance

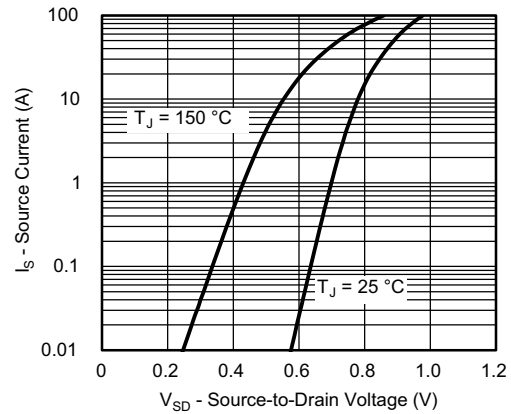


Gate Charge

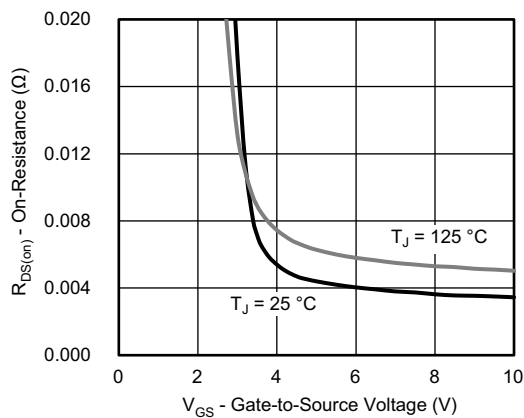
N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



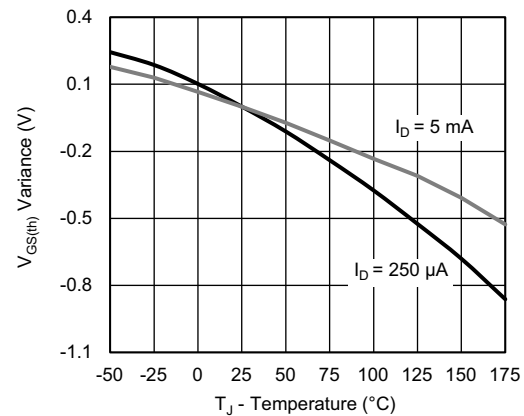
On-Resistance vs. Junction Temperature



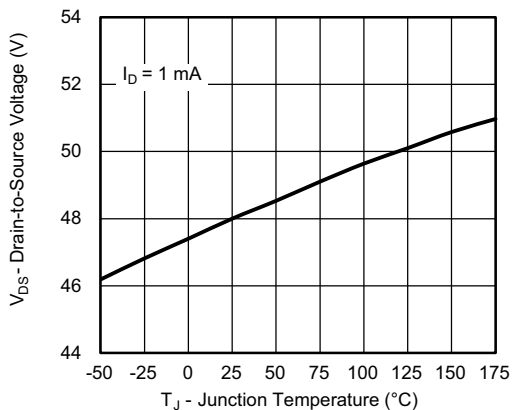
Source Drain Diode Forward Voltage



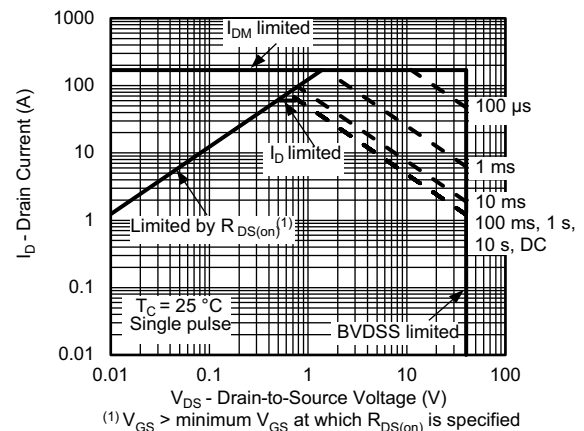
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

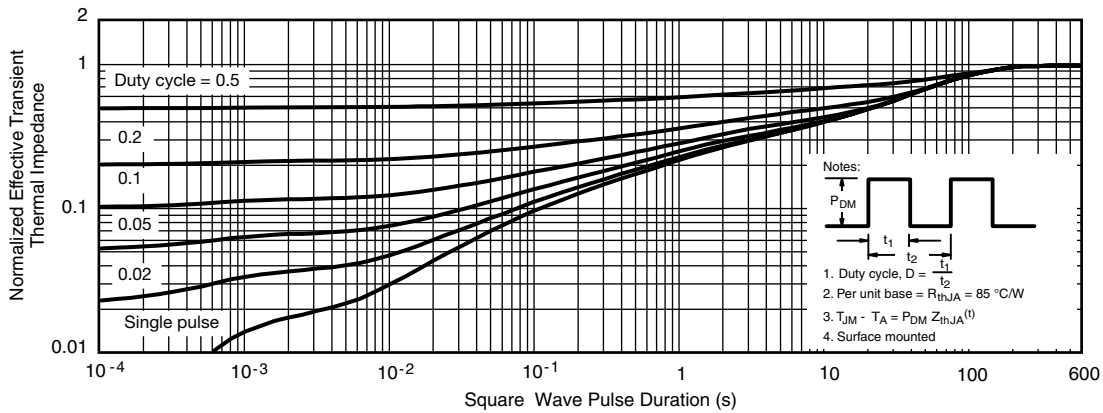


Drain Source Breakdown vs. Junction Temperature

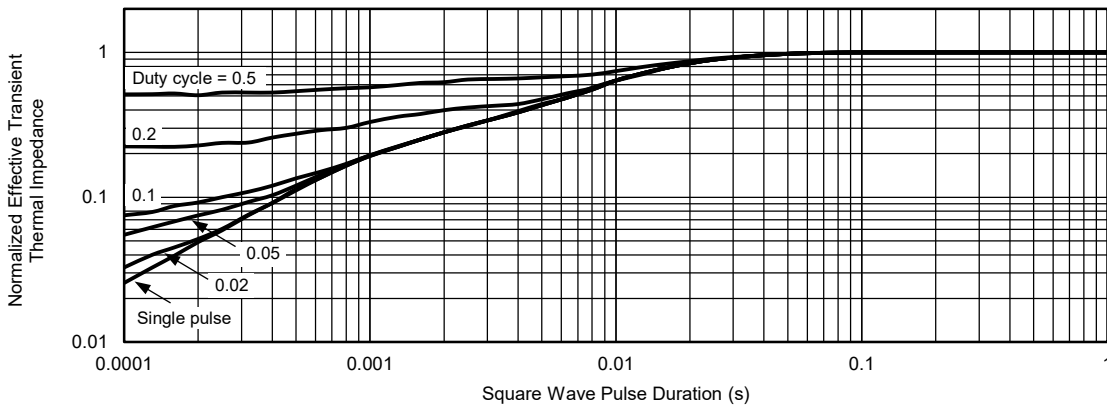


Safe Operating Area

N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the graph:
 - Normalized Transient Thermal Impedance Junction-to-Ambient ($25\text{ }^\circ\text{C}$) is given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76423.



PowerPAK[®] SO-8L Assymmetric Case Outline



| DIM. | MILLIMETERS | | | INCHES | | |
|------|-------------|------|------|--------|-------|-------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 1.00 | 1.07 | 1.14 | 0.039 | 0.042 | 0.045 |
| A1 | 0.00 | 0.06 | 0.13 | 0.000 | 0.003 | 0.005 |
| b | 0.33 | 0.41 | 0.48 | 0.013 | 0.016 | 0.019 |
| b1 | 0.44 | 0.51 | 0.58 | 0.017 | 0.020 | 0.023 |
| b2 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| b3 | 0.04 | 0.12 | 0.20 | 0.002 | 0.005 | 0.008 |
| c | 0.20 | 0.25 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 5.00 | 5.13 | 5.25 | 0.197 | 0.202 | 0.207 |
| D1 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| D2 | 3.63 | 3.73 | 3.83 | 0.143 | 0.147 | 0.151 |
| D3 | 0.81 | 0.91 | 1.01 | 0.032 | 0.036 | 0.040 |
| D4 | 1.98 | 2.08 | 2.18 | 0.078 | 0.082 | 0.086 |
| D5 | 1.47 | 1.57 | 1.67 | 0.058 | 0.062 | 0.066 |
| e | 1.20 | 1.27 | 1.34 | 0.047 | 0.050 | 0.053 |
| E | 6.05 | 6.15 | 6.25 | 0.238 | 0.242 | 0.246 |
| E1 | 4.27 | 4.37 | 4.47 | 0.168 | 0.172 | 0.176 |
| E2 | 2.75 | 2.85 | 2.95 | 0.108 | 0.112 | 0.116 |
| E3 | 1.89 | 1.99 | 2.09 | 0.074 | 0.078 | 0.082 |
| F | 0.05 | 0.12 | 0.19 | 0.002 | 0.005 | 0.007 |
| L | 0.62 | 0.72 | 0.82 | 0.024 | 0.028 | 0.032 |
| L1 | 0.92 | 1.07 | 1.22 | 0.036 | 0.042 | 0.048 |
| K | 0.41 | 0.51 | 0.61 | 0.016 | 0.020 | 0.024 |
| K1 | 0.64 | 0.74 | 0.84 | 0.025 | 0.029 | 0.033 |
| K2 | 0.54 | 0.64 | 0.74 | 0.021 | 0.025 | 0.029 |
| W | 0.13 | 0.23 | 0.33 | 0.005 | 0.009 | 0.013 |
| W1 | 0.31 | 0.41 | 0.51 | 0.012 | 0.016 | 0.020 |
| W2 | 2.72 | 2.82 | 2.92 | 0.107 | 0.111 | 0.115 |
| W3 | 2.86 | 2.96 | 3.06 | 0.113 | 0.117 | 0.120 |
| W4 | 0.41 | 0.51 | 0.61 | 0.016 | 0.020 | 0.024 |
| θ | 5° | 10° | 12° | 5° | 10° | 12° |

DWG: 6009

Note

- Millimeters will govern



RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8L DUAL ASYMMETRIC



Recommended Minimum Pads
Dimensions in mm [inches]



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Vishay products are not designed for use in life-saving or life-sustaining applications or any application in which the failure of the Vishay product could result in personal injury or death unless specifically qualified in writing by Vishay. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.