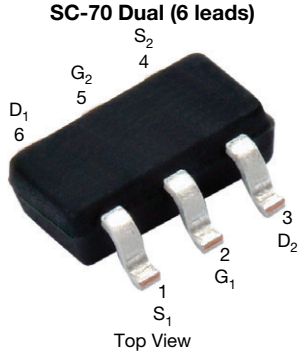
# Automotive Dual N-Channel 20 V (D-S) 175 °C MOSFET

**SOT-363**
**SC-70 Dual (6 leads)**




Top View

**Marking Code**: 8T

## FEATURES

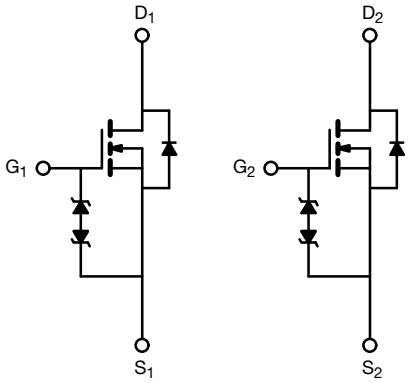
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % $R_g$ tested
- Typical ESD protection: 800 V
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

RoHS COMPLIANT

HALOGEN FREE




| PRODUCT SUMMARY | |
|---|---|
| $V_{DS}$ (V) | 20 |
| $R_{DS(on)}$ (Ω) at $V_{GS}$ = 4.5 V | 0.300 |
| $I_D$ (A) per leg | 0.85 |
| Configuration | Dual |
| Package | SC-70 |

**ABSOLUTE MAXIMUM RATINGS** ($T_C$ = 25 °C, unless otherwise noted)

| PARAMETER | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DS}$ | 20 | V |
| Gate-source voltage | | $V_{GS}$ | ± 12 | |
| Continuous drain current [a] | $T_C$ = 25 °C | $I_D$ | 0.85 | A |
| | $T_C$ = 125 °C | | 0.53 | |
| Continuous source current (diode conduction) [a] | | $I_S$ | 0.63 | |
| Pulsed drain current [b] | | $I_{DM}$ | 3.3 | |
| Single Pulse Avalanche Current | L = 0.1 mH | $I_{AS}$ | 2 | |
| Single Pulse Avalanche Energy | | $E_{AV}$ | 0.2 | mJ |
| Maximum power dissipation [b] | $T_C$ = 25 °C | $P_D$ | 1.5 | W |
| | $T_C$ = 125 °C | | 0.5 | |
| Operating junction and storage temperature range | | $T_J$, $T_{stg}$ | -55 to +175 | °C |

**THERMAL RESISTANCE RATINGS**

| PARAMETER | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|
| Junction-to-ambient | PCB mount [c] | $R_{thJA}$ | 460 | °C/W |
| Junction-to-foot (drain) | | $R_{thJF}$ | 350 | |

**Notes**

a. Package limited
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
c. When mounted on 1" square PCB (FR4 material)

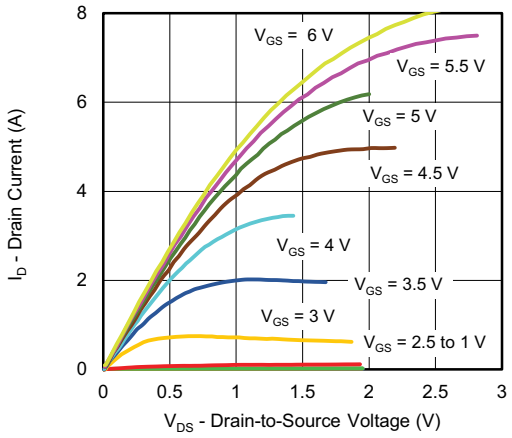
| **SPECIFICATIONS** ($T_C$ = 25 °C, unless otherwise noted) | | | | | | | |
|---|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | | |
| Drain-source breakdown voltage | $V_{DS}$ | $V_{GS}$ = 0, $I_D$ = 250 µA | | 20 | - | - | V |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | | 1.5 | 2 | 2.5 | |
| Gate-source leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 3 V | | - | - | ± 1 | µA |
| | | $V_{DS}$ = 0 V, $V_{GS}$ = ± 12 V | | - | - | ± 10 | mA |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{GS}$ = 0 V | $V_{DS}$ = 20 V | - | - | 1 | µA |
| | | $V_{GS}$ = 0 V | $V_{DS}$ = 20 V, $T_J$ = 125 °C | - | - | 50 | |
| | | $V_{GS}$ = 0 V | $V_{DS}$ = 20 V, $T_J$ = 175 °C | - | - | 150 | |
| On-state drain current [a] | $I_{D(on)}$ | $V_{GS}$ = 4.5 V | $V_{DS}$ ≥ 5 V | 0.4 | - | - | A |
| Drain-source on-state resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = 4.5 V | $I_D$ = 0.4 A | - | 0.210 | 0.300 | Ω |
| | | $V_{GS}$ = 4.5 V | $I_D$ = 0.4 A, $T_J$ = 125 °C | - | - | 0.490 | |
| | | $V_{GS}$ = 4.5 V | $I_D$ = 0.4 A, $T_J$ = 175°C | - | - | 0.530 | |
| **Dynamic [b]** | | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{GS}$ = 0 V | $V_{DS}$ = 10 V, f = 1 MHz | - | 60 | - | pF |
| Output capacitance | $C_{oss}$ | | | - | 26 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | | - | 15 | - | |
| Total gate charge [c] | $Q_g$ | $V_{GS}$ = 4.5 V | $V_{DS}$ = 10 V, $I_D$ = 1.2 A | - | 0.9 | 1.2 | nC |
| Gate-source charge [c] | $Q_{gs}$ | | | - | 0.5 | - | |
| Gate-drain charge [c] | $Q_{gd}$ | | | - | 0.3 | - | |
| Gate resistance [d] | $R_g$ | f = 1 MHz | | 5 | 8.5 | 13.5 | Ω |
| Turn-on delay time [c] | $t_{d(on)}$ | $V_{DD}$ = 10 V, $R_L$ = 20 Ω<br>$I_D$ ≅ 0.5 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 Ω | | - | 10 | 15 | ns |
| Rise time [c] | $t_r$ | | | - | 9.6 | 15 | |
| Turn-off delay time [c] | $t_{d(off)}$ | | | - | 8 | 12 | |
| Fall time [c] | $t_f$ | | | - | 6 | 10 | |
| **Source-Drain Diode Ratings and Characteristics [b]** | | | | | | | |
| Pulsed current [a] | $I_{SM}$ | | | - | - | 3 | A |
| Forward voltage | $V_{SD}$ | $I_F$ = 0.5 A, $V_{GS}$ = 0 | | - | 0.8 | 1.2 | V |

**Notes**

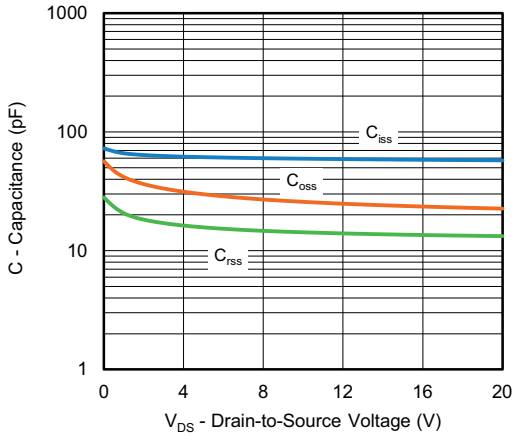
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature
d. Gate is obscured by ESD network series resistance and cannot be tested directly

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

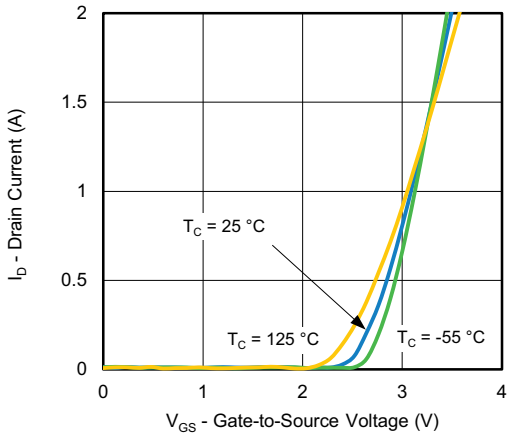
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



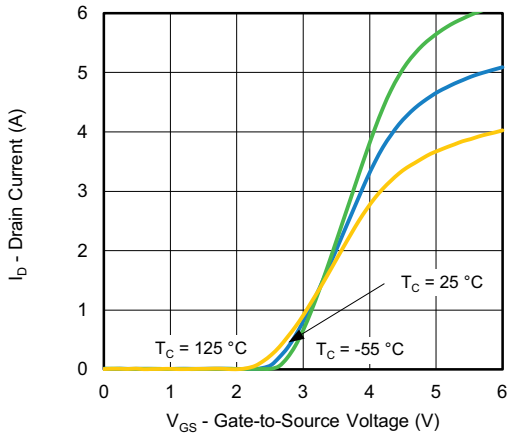

**Output Characteristics**



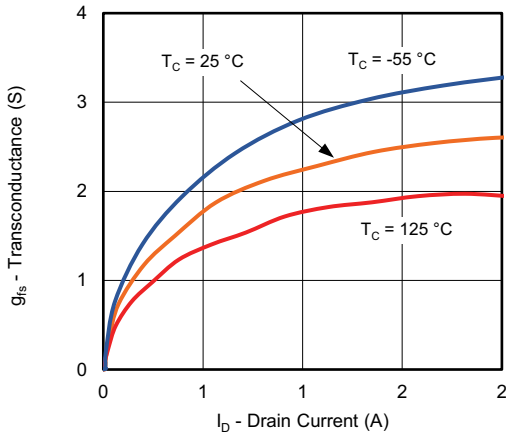

**Capacitance**



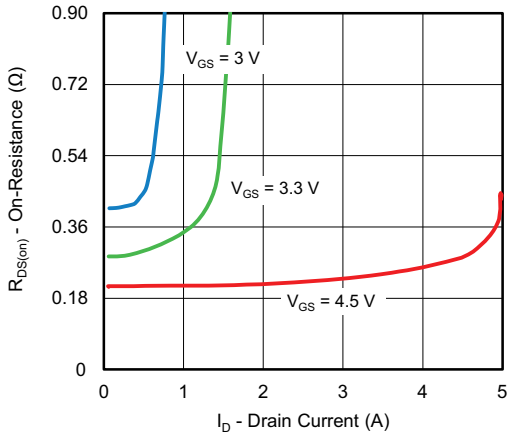

**Transfer Characteristics**




**Transfer Characteristics**

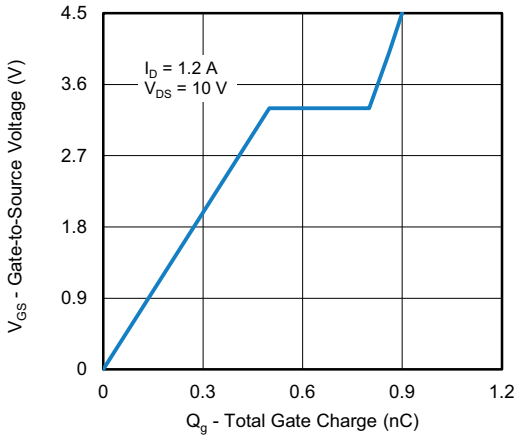



**Transconductance**

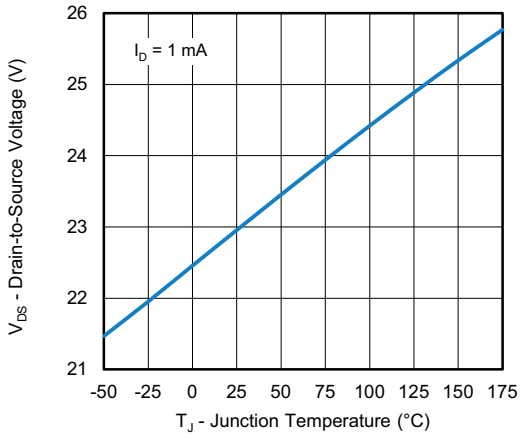



**On-Resistance vs. Drain Current**

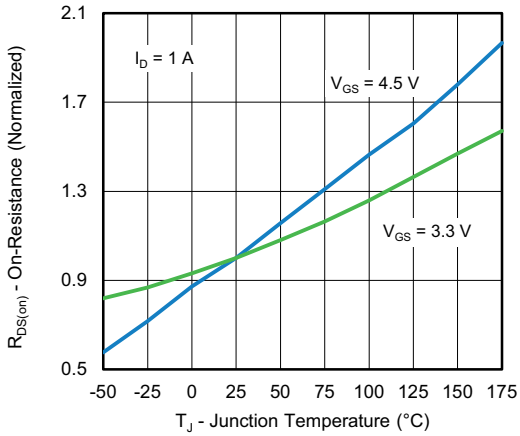
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



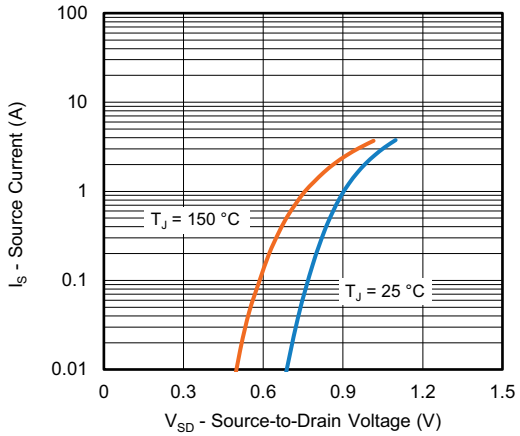

**Gate Charge**



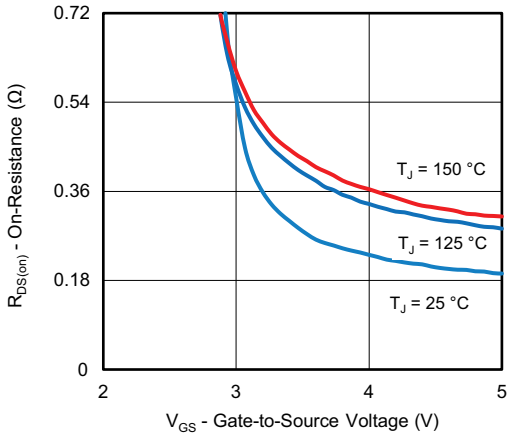

**Drain Source Breakdown vs. Junction Temperature**



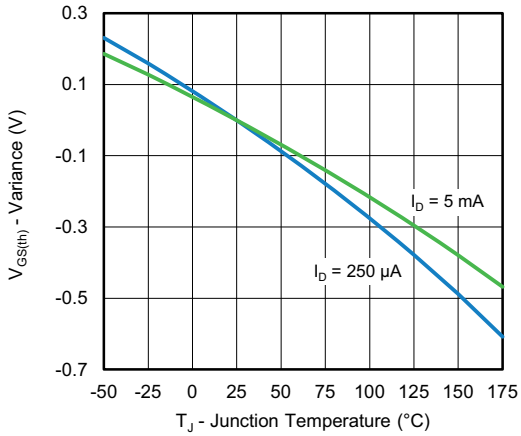

**On-Resistance vs. Junction Temperature**




**Source Drain Diode Forward Voltage**

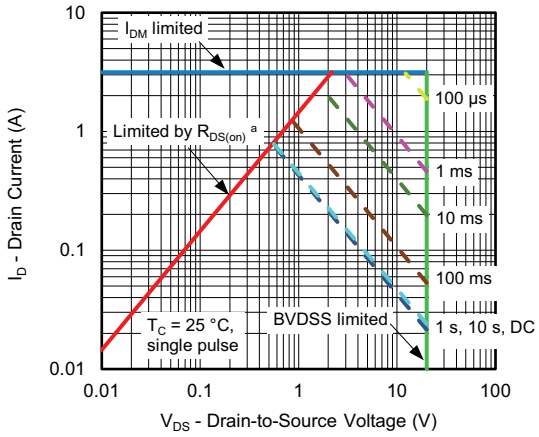



**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**

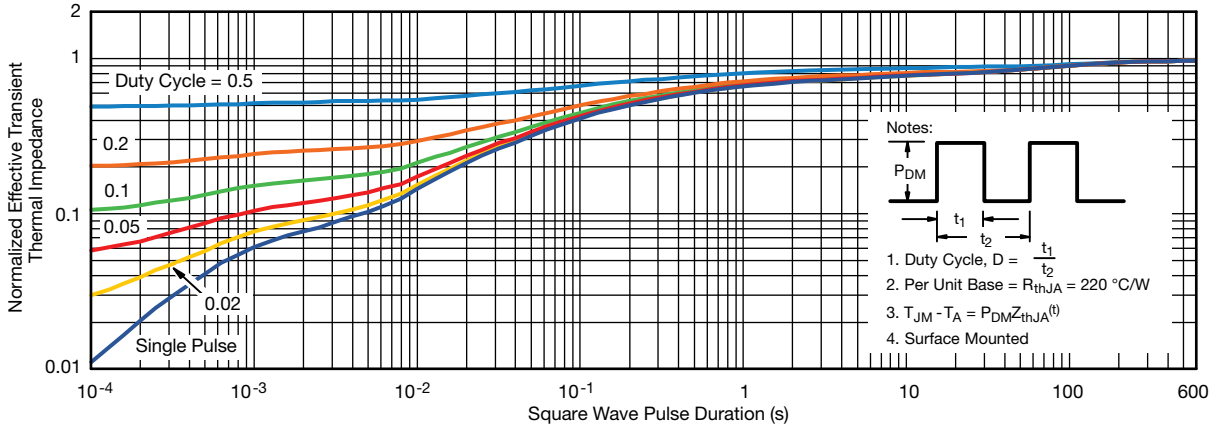
**THERMAL RATINGS** ($T_A$ = 25 °C, unless otherwise noted)




**Safe Operating Area**

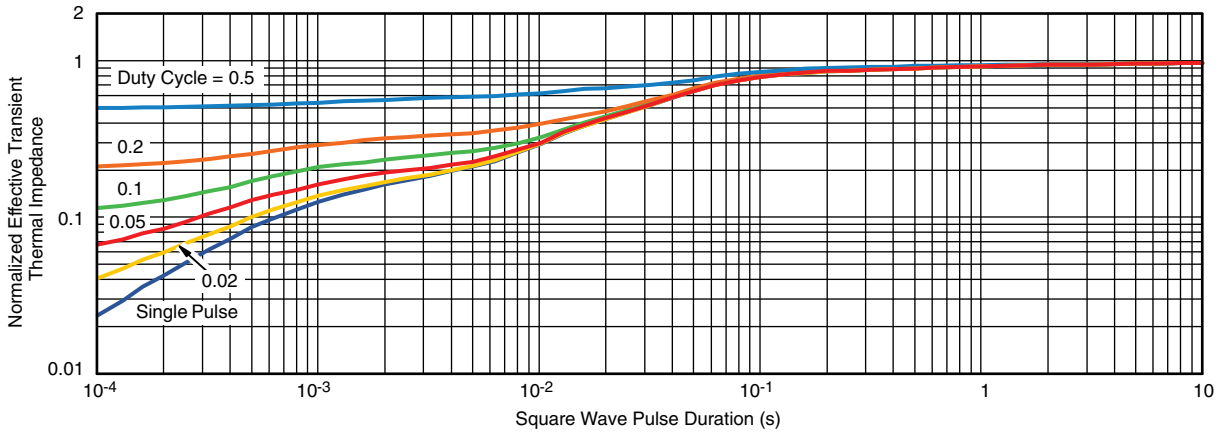
**Note**

a. $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified




**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**THERMAL RATINGS** ($T_A$ = 25 °C, unless otherwise noted)




**Normalized Thermal Transient Impedance, Junction-to-Foot**

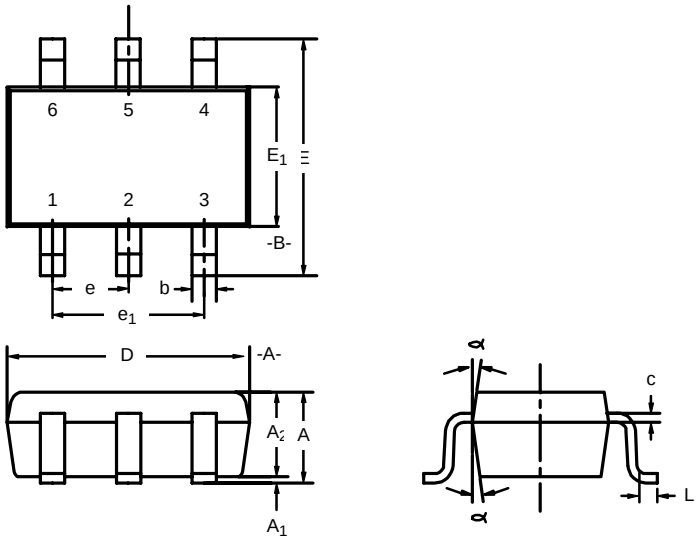
**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76699.*

## SC-70: 6-LEADS




| Dim | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | Min | Nom | Max | Min | Nom | Max |
| **A** | 0.90 | – | 1.10 | 0.035 | – | 0.043 |
| **$A_1$** | – | – | 0.10 | – | – | 0.004 |
| **$A_2$** | 0.80 | – | 1.00 | 0.031 | – | 0.039 |
| **b** | 0.15 | – | 0.30 | 0.006 | – | 0.012 |
| **c** | 0.10 | – | 0.25 | 0.004 | – | 0.010 |
| **D** | 1.80 | 2.00 | 2.20 | 0.071 | 0.079 | 0.087 |
| **E** | 1.80 | 2.10 | 2.40 | 0.071 | 0.083 | 0.094 |
| **$E_1$** | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| **e** | 0.65BSC | | | 0.026BSC | | |
| **$e_1$** | 1.20 | 1.30 | 1.40 | 0.047 | 0.051 | 0.055 |
| **L** | 0.10 | 0.20 | 0.30 | 0.004 | 0.008 | 0.012 |
| **α** | 7°Nom | | | 7°Nom | | |

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DWG: 5550

# Dual-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Recommended Pad Pattern and Thermal Performance

## INTRODUCTION

This technical note discusses the pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for dual-channel LITTLE FOOT power MOSFETs in the SC-70 package. These new Vishay Siliconix devices are intended for small-signal applications where a miniaturized package is needed and low levels of current (around 250 mA) need to be switched, either directly or by using a level shift configuration. Vishay provides these devices with a range of on-resistance specifications in 6-pin versions. The new 6-pin SC-70 package enables improved on-resistance values and enhanced thermal performance.

## PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration.

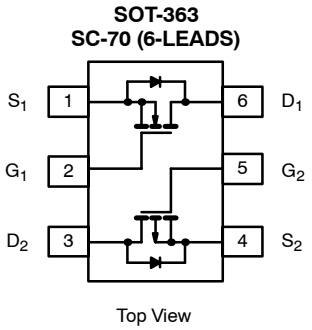



**FIGURE 1.**

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

## BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the 6-pin SC-70. This basic pad pattern is sufficient for the low-power applications for which this package is intended. For the 6-pin device, increasing the pad patterns yields a reduction in thermal resistance on the order of 20% when using a 1-inch square with full copper on both sides of the printed circuit board (PCB).

## EVALUATION BOARDS FOR THE DUAL SC70-6

The 6-pin SC-70 evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows interrogation from the outer pins to 6-pin DIP connections permitting test sockets to be used in evaluation testing.

The thermal performance of the dual SC-70 has been measured on the EVB with the results shown below. The minimum recommended footprint on the evaluation board was compared with the industry standard 1-inch square FR4 PCB with copper on both sides of the board.

## THERMAL PERFORMANCE

### Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package measured as junction-to-foot thermal resistance is 300°C/W typical, 350°C/W maximum. The “foot” is the drain lead of the device as it connects with the body. Note that these numbers are somewhat higher than other LITTLE FOOT devices due to the limited thermal performance of the Alloy 42 lead-frame compared with a standard copper lead-frame.

### Junction-to-Ambient Thermal Resistance (dependent on PCB size)

The typical $R\theta_{JA}$ for the dual 6-pin SC-70 is 400°C/W steady state. Maximum ratings are 460°C/W for the dual. All figures based on the 1-inch square FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at two different ambient temperatures.

| SC-70 (6-PIN) | |
|---|---|
| **Room Ambient 25 °C** | **Elevated Ambient 60 °C** |
| $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ | $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ |
| $P_D = \frac{150°C - 25°C}{400°C/W}$ | $P_D = \frac{150°C - 60°C}{400°C/W}$ |
| $P_D$ = 312 mW | $P_D$ = 225 mW |

NOTE: Although they are intended for low-power applications, devices in the 6-pin SC-70 will handle power dissipation in excess of 0.2 W.

### Testing

To aid comparison further, Figure 2 illustrates the dual-channel SC-70 thermal performance on two different board sizes and two different pad patterns. The results display the thermal performance out to steady state. The measured steady state values of $R\theta_{JA}$ for the dual 6-pin SC-70 are as follows:

| LITTLE FOOT SC-70 (6-PIN) | |
|---|---|
| 1) Minimum recommended pad pattern (see Figure 2) on the EVB of 0.5 inches x 0.6 inches. | 518°C/W |
| 2) Industry standard 1" square PCB with maximum copper both sides. | 413°C/W |

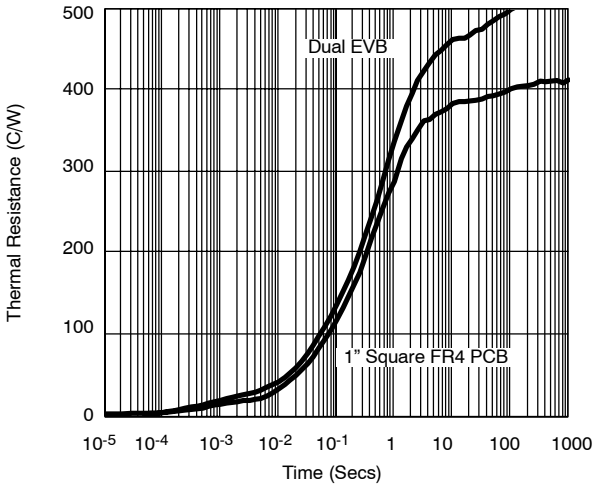



**FIGURE 2.** Comparison of Dual SC70-6 on EVB and 1" Square FR4 PCB.

The results show that if the board area can be increased and maximum copper traces are added, the thermal resistance reduction is limited to 20%. This fact confirms that the power dissipation is restricted with the package size and the Alloy 42 leadframe.

## ASSOCIATED DOCUMENT

Single-Channel LITTLE FOOT SC-70 6-Pin MOSFET Copper Leadframe Version, REcommended Pad Pattern and Thermal Performance, AN815, (http://www.vishay.com/doc?71334).

# Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

## INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

## PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n-and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.

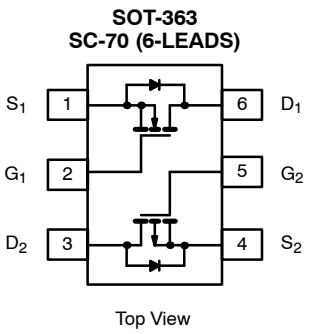



**FIGURE 1.**

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

## BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (Figure 2) yields a reduction in thermal resistance and is a preferred footprint.

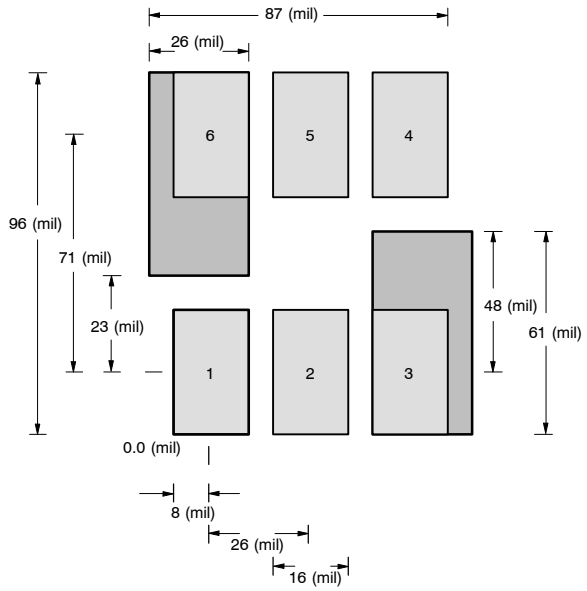



**FIGURE 2.** SC-70 (6 leads) Dual

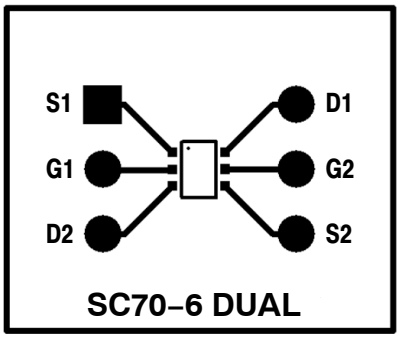
## EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in Figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, *Basic Pad Patterns*. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch$^2$ PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.

Front of Board SC70-6




Back of Board SC70-6

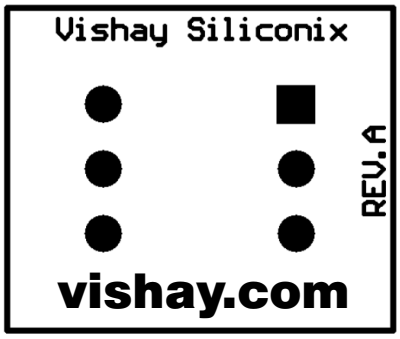



**FIGURE 3.**

## THERMAL PERFORMANCE

### Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the "foot" is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80°C/W, with a maximum thermal resistance of approximately 100°C/W. This data compares favorably with another compact, dual-channel package – the dual TSOP-6 – which features a typical thermal resistance of 75°C/W and a maximum of 90°C/W.

### Power Dissipation

The typical $R\theta_{JA}$ for the dual-channel 6-pin SC-70 with a copper leadframe is 224°C/W steady-state, compared to 413°C/W for the Alloy 42 version. All figures are based on the 1-inch$^2$ FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at varying ambient temperatures.

*Alloy 42 Leadframe*

| ALLOY 42 LEADFRAME | |
|---|---|
| **Room Ambient 25 °C** | **Elevated Ambient 60 °C** |
| $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ | $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ |
| $P_D = \frac{150^oC - 25^oC}{413^oC/W}$ | $P_D = \frac{150^oC - 60^oC}{413^oC/W}$ |
| $P_D$ = 303 mW | $P_D$ = 218 mW |

| COOPER LEADFRAME | |
|---|---|
| **Room Ambient 25 °C** | **Elevated Ambient 60 °C** |
| $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ | $P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$ |
| $P_D = \frac{150^oC - 25^oC}{224^oC/W}$ | $P_D = \frac{150^oC - 60^oC}{224^oC/W}$ |
| $P_D$ = 558 mW | $P_D$ = 402 mW |

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

## TESTING

To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of $R\theta_{JA}$ for the dual 6-pin SC-70 with varying leadframes are as follows:

| LITTLE FOOT 6-PIN SC-70 | | |
|---|---|---|
| | **Alloy 42** | **Copper** |
| 1) Minimum recommended pad pattern on the EVB board (see Figure 3). | 518°C/W | 344°C/W |
| 2) Industry standard 1-inch$^2$ PCB with maximum copper both sides. | 413°C/W | 224°C/W |

The results indicate that designers can reduce thermal resistance (θJA) by 34% simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174°C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120°C/W reduction can be obtained by utilizing a 1-inch$^2$. PCB area.

The Dual copper leadframe versions have the following suffix:

| | |
|---|---|
| Dual: | Si19xxEDH |
| Compl.: | Si15xxEDH |

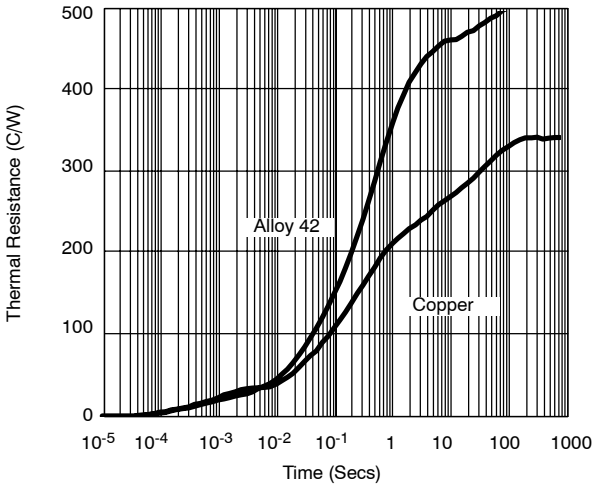



**FIGURE 4.** Dual SC70-6 Thermal Performance on EVB

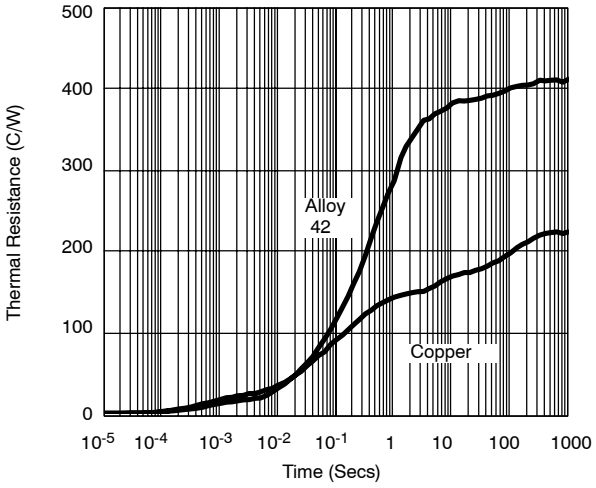
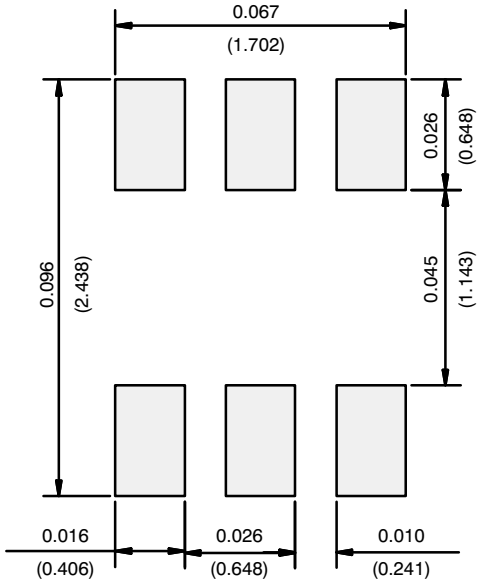



**FIGURE 5.** Dual SC70-6 Comparison on 1-inch$^2$ PCB

## RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead




Recommended Minimum Pads
Dimensions in Inches/(mm)

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# Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance 175 °C Rated Part

## INTRODUCTION

The new dual 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the dual-channel version.

## PIN-OUT

Figure 1 shows the pin-out description and pin 1 identification for the dual-channel SC-70 device in the 6-pin configuration. Both n-and p-channel devices are available in this package – the drawing example below illustrates the p-channel device.

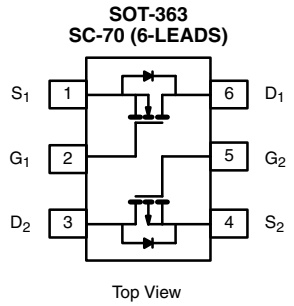



Fig. 1

For package dimensions see outline drawing SC-70 (6-Leads) (www.vishay.com/doc?71154)

## BASIC PAD PATTERNS

See Application Note 826, Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs, (www.vishay.com/doc?72286) for the SC-70 6-pin basic pad layout and dimensions. This pad pattern is sufficient for the low-power applications for which this package is intended. Increasing the drain pad pattern (figure 2) yields a reduction in thermal resistance and is a preferred footprint.

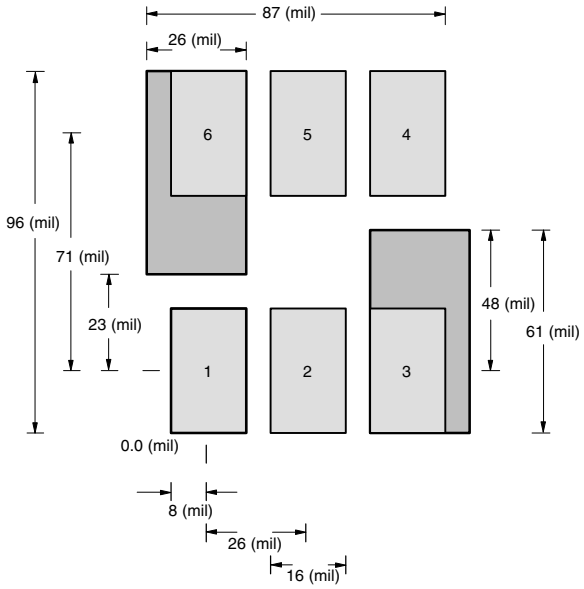



Fig. 2 SC-70 (6 leads) Dual

## EVALUATION BOARD FOR THE DUAL-CHANNEL SC70-6

The 6-pin SC-70 evaluation board (EVB) shown in figure 3 measures 0.6 in. by 0.5 in. The copper pad traces are the same as described in the previous section, Basic Pad Patterns. The board allows for examination from the outer pins to the 6-pin DIP connections, permitting test sockets to be used in evaluation testing.

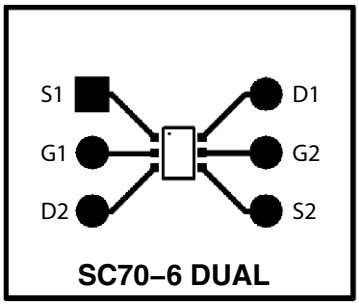
The thermal performance of the dual 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was then repeated using the 1-inch$^2$ PCB with dual-side copper coating.

A helpful way of displaying the thermal performance of the 6-pin SC-70 dual copper leadframe is to compare it to the traditional Alloy 42 version.

APPLICATION NOTE

# Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance 175 °C Rated Part

Front of Board SC70-6




Back of Board SC70-6

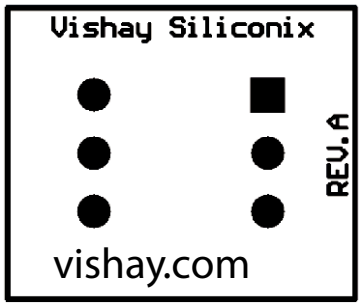



Fig. 3

## THERMAL PERFORMANCE

### Junction-to-Foot Thermal Resistance (the Package Performance)

Thermal performance for the dual SC-70 6-pin package is measured as junction-to-foot thermal resistance, in which the “foot” is the drain lead of the device as it connects with the body. The junction-to-foot thermal resistance for this device is typically 80 °C/W, with a maximum thermal resistance of approximately 100 °C/W. This data compares favorably with another compact, dual-channel package - the dual TSOP-6 - which features a typical thermal resistance of 75 °C/W and a maximum of 90 °C/W.

### Power Dissipation for 175 °C Rated Part

The typical RθJA for the dual-channel 6-pin SC-70 with a copper leadframe is 224 °C/W steady-state, compared to 413 °C/W for the Alloy 42 version. All figures are based on the 1-inch$^2$ FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the dual 6-pin SC-70 package at varying ambient temperatures.

### Alloy 42 Leadframe

| ALLOY 42 LEADFRAME | |
|---|---|
| ROOM AMBIENT 25 °C | ELEVATED AMBIENT 60 °C |
| $P_D = \frac{T_{J(max.)} - T_A}{R\theta_{JA}}$ | $P_D = \frac{T_{J(max.)} - T_A}{R\theta_{JA}}$ |
| $P_D = \frac{175\ °C - 25\ °C}{413\ °C/W}$ | $P_D = \frac{175\ °C - 60\ °C}{413\ °C/W}$ |
| $P_D = 363\ mW$ | $P_D = 278\ mW$ |

| COOPER LEADFRAME | |
|---|---|
| ROOM AMBIENT 25 °C | ELEVATED AMBIENT 60 °C |
| $P_D = \frac{T_{J(max.)} - T_A}{R\theta_{JA}}$ | $P_D = \frac{T_{J(max.)} - T_A}{R\theta_{JA}}$ |
| $P_D = \frac{175\ °C - 25\ °C}{224\ °C/W}$ | $P_D = \frac{175\ °C - 60\ °C}{224\ °C/W}$ |
| $P_D = 669\ mW$ | $P_D = 513\ mW$ |

Although they are intended for low-power applications, devices in the 6-pin SC-70 dual-channel configuration will handle power dissipation in excess of 0.5 W.

## TESTING

To further aid the comparison of copper and Alloy 42 leadframes, Figures 4 and 5 illustrate the dual-channel 6-pin SC-70 thermal performance on two different board sizes and pad patterns. The measured steady-state values of $R\theta_{JA}$ for the dual 6-pin SC-70 with varying leadframes are as follows:

| LITTLE FOOT 6-PIN SC-70 | | |
|---|---|---|
| | ALLOY 42 | COPPER |
| 1) Minimum recommended pad pattern on the EVB board (see fig. 3). | 518 °C/W | 344 °C/W |
| 2) Industry standard 1-inch$^2$ PCB with maximum copper both sides. | 413 °C/W | 224 °C/W |

The results indicate that designers can reduce thermal resistance ($\theta_{JA}$) by 34 % simply by using the copper leadframe device as opposed to the Alloy 42 version. In this example, a 174 °C/W reduction was achieved without an increase in board area. If an increase in board size is feasible, a further 120 °C/W reduction can be obtained by utilizing a 1-inch$^2$. PCB area.

APPLICATION NOTE

# Dual-Channel LITTLE FOOT® 6-Pin SC-70 MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance 175 °C Rated Part

The dual copper leadframe versions have the following suffix:

| | |
|---|---|
| Dual: | Sx19xxEDH or Sx19xxEEH |
| Compl.: | Sx15xxEDH or Sx15xxEEH |

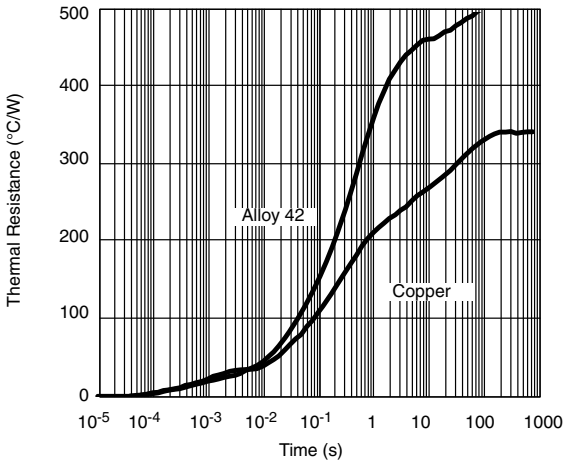



Fig. 4 Dual SC70-6 Thermal Performance on EVB

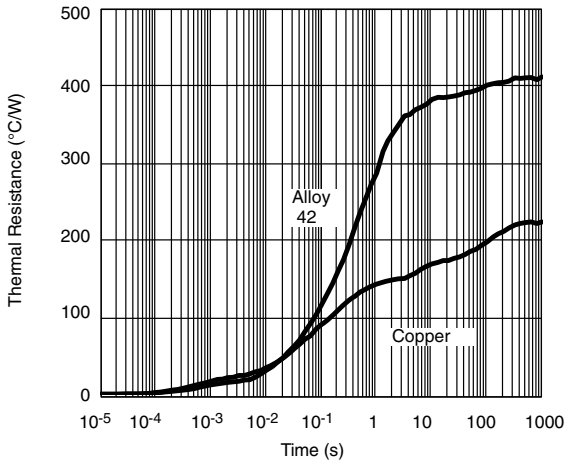



Fig. 5 Dual SC70-6 Comparison on 1-inch$^2$ PCB

APPLICATION NOTE

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