# N-Channel 100 V (D-S) MOSFET

## DESCRIPTION

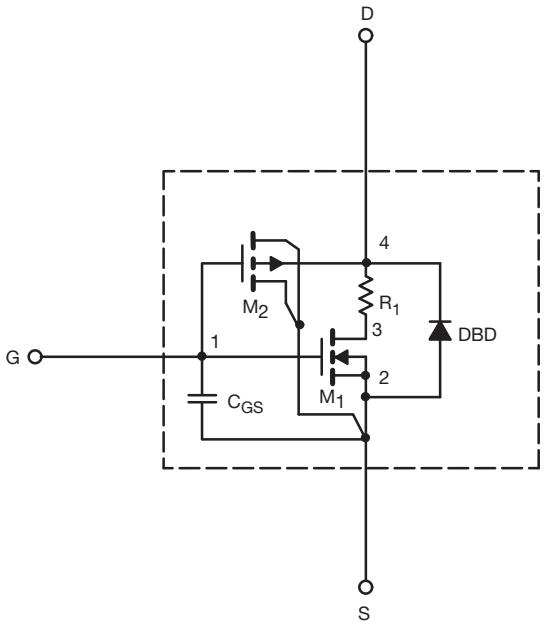
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- Model the Gate Charge

## SUBCIRCUIT MODEL SCHEMATIC




**Note**

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



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| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **SIMULATED DATA** | **MEASURED DATA** | **UNIT** |
| **Static** | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 2.4 | - | V |
| On-State Drain Current [a] | $I_{D(on)}$ | $V_{DS}$ = 5 V, $V_{GS}$ = 10 V | 408 | - | A |
| Drain-Source On-State Resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 30 A | 0.012 | 0.012 | Ω |
| | | $V_{GS}$ = 10 V, $I_D$ = 30 A, $T_J$ = 125 °C | 0.018 | - | |
| | | $V_{GS}$ = 10 V, $I_D$ = 30 A, $T_J$ = 175 °C | 0.021 | - | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 20 A | 0.014 | 0.014 | |
| Diode Forward Voltage [a] | $V_{SD}$ | $I_F$ = 60 A, $V_{GS}$ = 0 V | 0.91 | 1 | V |
| Dynamic [b] | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 25 V, $V_{GS}$ = 0 V, f = 1 MHz | 3874 | 3820 | pF |
| Output Capacitance | $C_{oss}$ | | 475 | 450 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 212 | 210 | |
| Total Gate Charge [c] | $Q_g$ | $V_{DS}$ = 50 V, $V_{GS}$ = 10 V, $I_D$ = 60 A | 72.5 | 73 | nC |
| Gate-Source Charge [c] | $Q_{gs}$ | | 15 | 15 | |
| Gate-Drain Charge [c] | $Q_{gd}$ | | 20 | 20 | |
| Turn-On Delay Time [c] | $t_{d(on)}$ | $V_{DD}$ = 50 V, $R_L$ = 0.83 Ω<br>$I_D$ = 60 A, $V_{GEN}$ = 10 V, $R_g$ = 2.5 Ω | 10 | 12 | ns |
| Rise Time [c] | $t_r$ | | 56 | 90 | |
| Turn-Off Delay Time [c] | $t_{d(off)}$ | | 54 | 55 | |
| Fall Time [c] | $t_f$ | | 24 | 130 | |

**Notes**

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.


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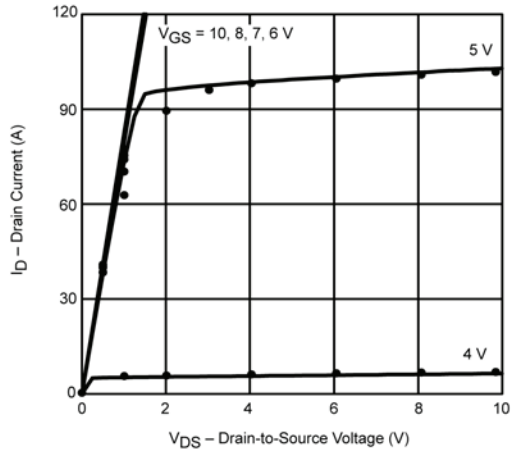
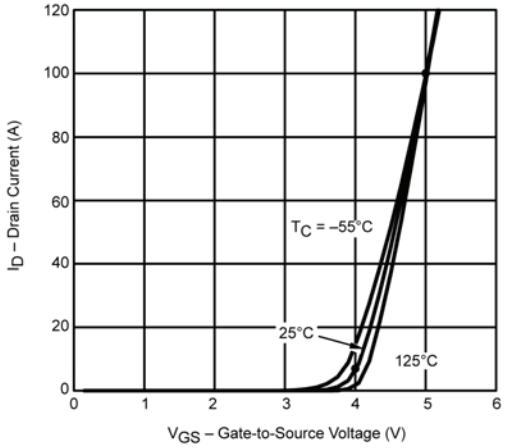
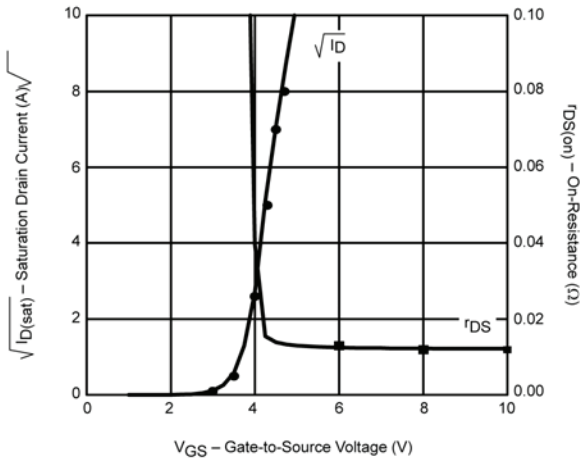
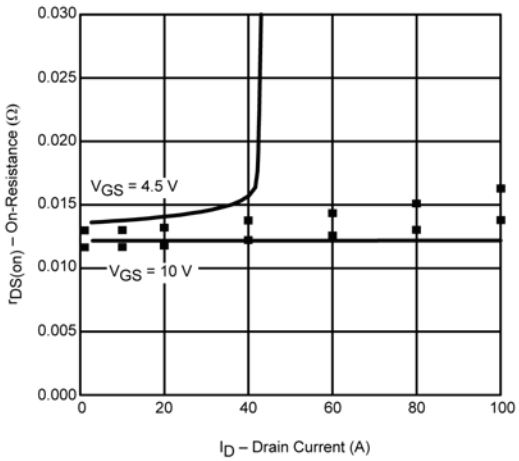
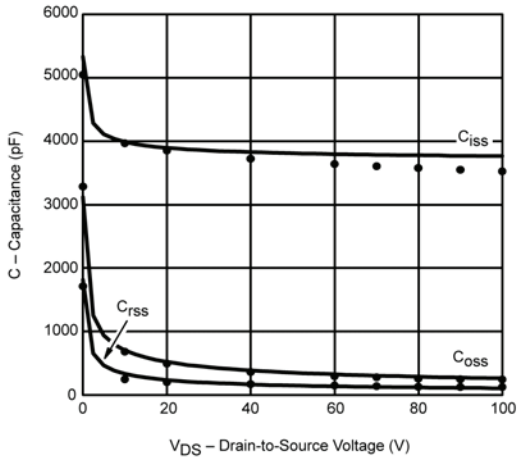
## COMPARISON OF MODEL WITH MEASURED DATA ($T_J$ = 25 °C, unless otherwise noted)

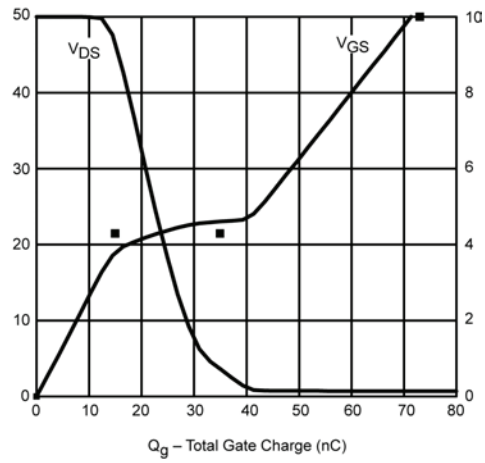



**Note**

- Dots and squares represent measured data.

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