Dual N-Channel 30 V (D-S) MOSFET with Schottky Diode

DESCRIPTION

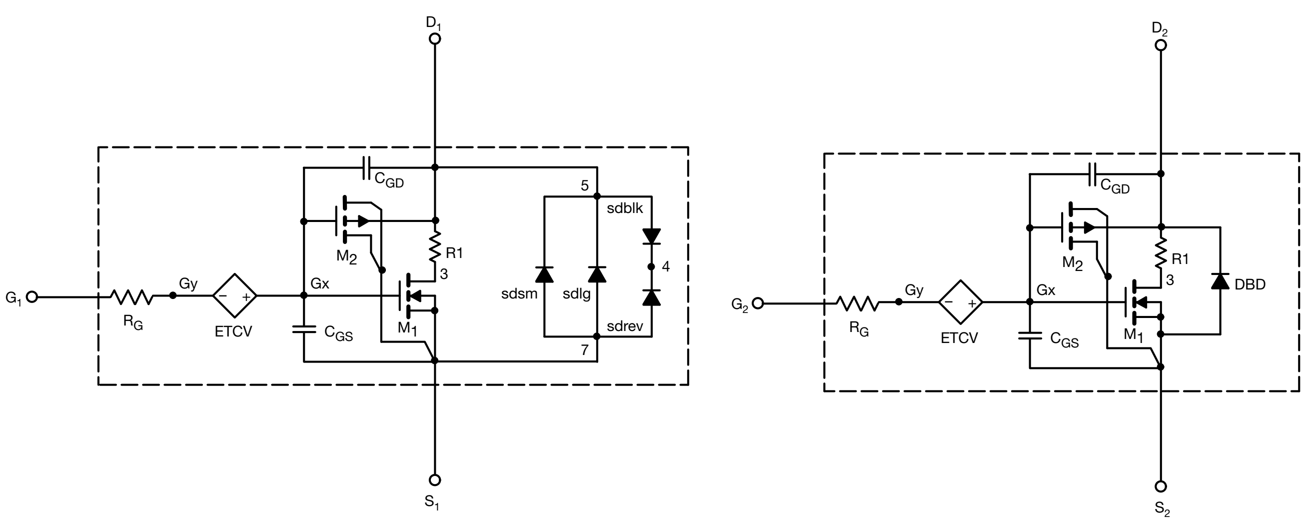
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (Sub-circuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over the -55 °C to +125 °C temperature range
- Model the gate charge

SUB-CIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**SIMULATED DATA**	**MEASURED DATA**	**UNIT**
Static						
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 μA	Ch-1	1.6	-	V
			Ch-2	1.6	-	
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 15 A	Ch-1	0.0048	0.0047	Ω
		V_{GS} = 10 V, I_D = 19 A	Ch-2	0.0022	0.0022	
		V_{GS} = 4.5 V, I_D = 12 A	Ch-1	0.0068	0.0065	
		V_{GS} = 4.5 V, I_D = 15 A	Ch-2	0.0030	0.0030	
Forward Transconductance [a]	g_{fs}	V_{DS} = 10 V, I_D = 15 A	Ch-1	92	80	S
		V_{DS} = 10 V, I_D = 19 A	Ch-2	162	165	
Diode Forward Voltage [a]	V_{SD}	I_S = 10 A, V_{GS} = 0 V	Ch-1	0.80	0.80	V
		I_S = 2 A, V_{GS} = 0 V	Ch-2	0.41	0.41	
Dynamic [b]						
Input Capacitance	C_{iss}	Channel-1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz Channel-2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Ch-1	929	930	pF
			Ch-2	2460	2620	
Output Capacitance	C_{oss}		Ch-1	340	325	
			Ch-2	943	902	
Reverse Transfer Capacitance	C_{rss}		Ch-1	23	21	
			Ch-2	47	55	
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 20 A	Ch-1	12	12	nC
			Ch-2	30	29.5	
		Channel-1 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A Channel-2 V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 20 A	Ch-1	5.6	5.4	
			Ch-2	14	13.2	
Gate-Source Charge	Q_{gs}		Ch-1	3	3	
			Ch-2	7.1	7.1	
Gate-Drain Charge	Q_{gd}		Ch-1	0.75	0.75	
			Ch-2	1.3	1.3	

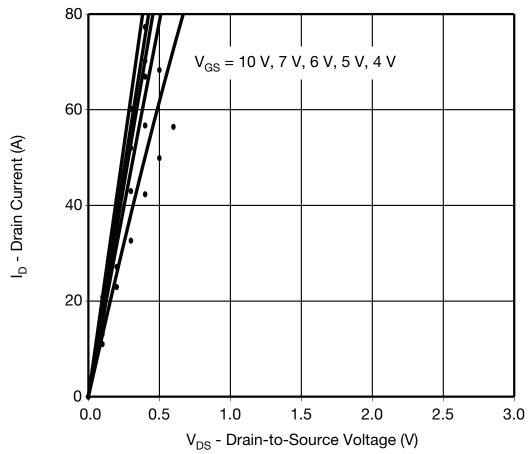
Notes

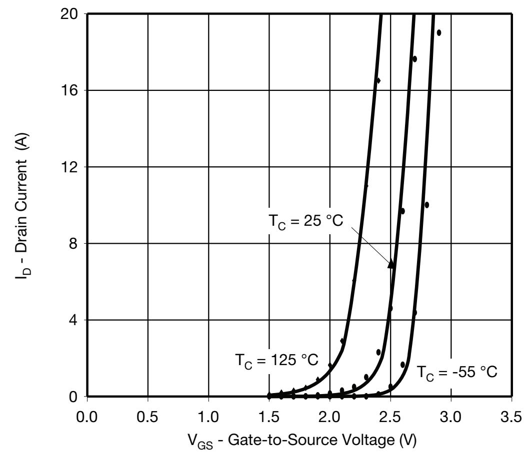
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

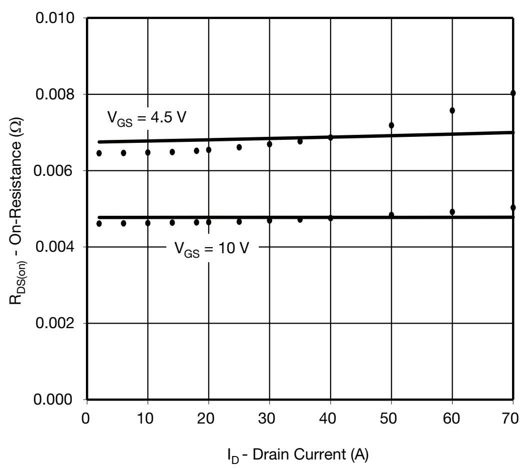
b. Guaranteed by design, not subject to production testing.

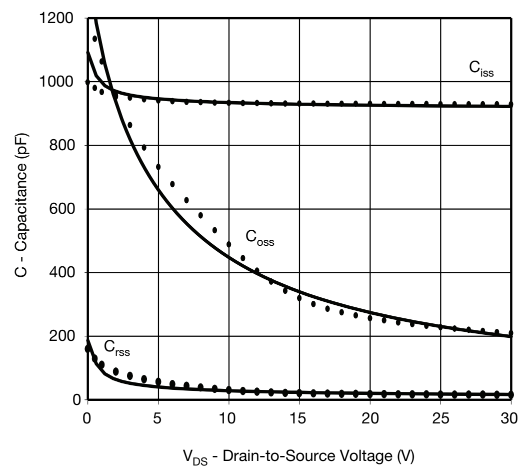
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

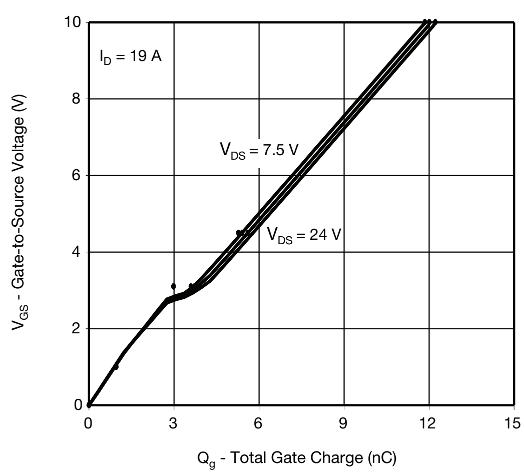
N-Channel 1

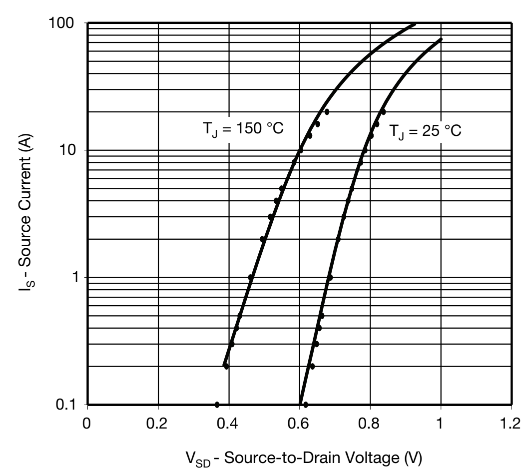










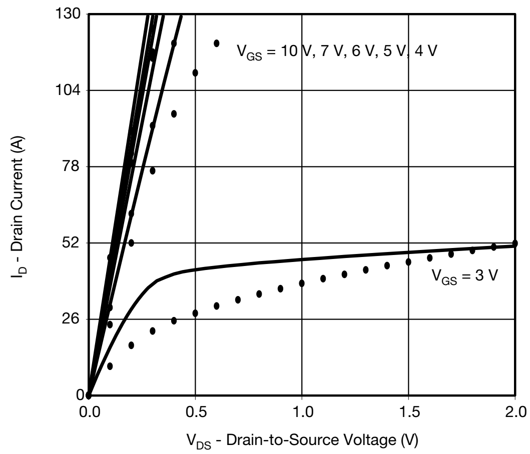


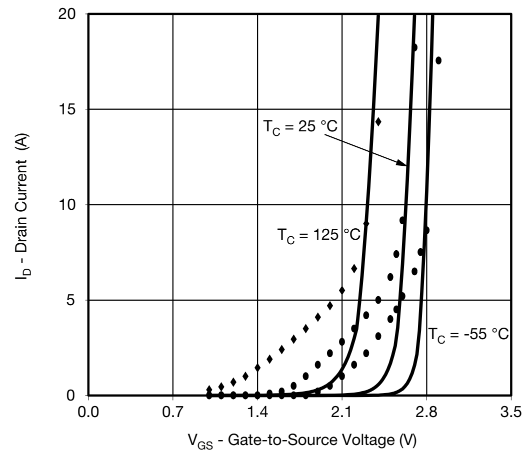
Note

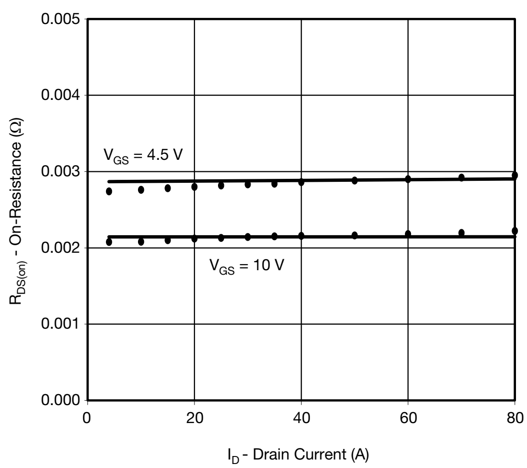
- Dots and squares represent measured data.

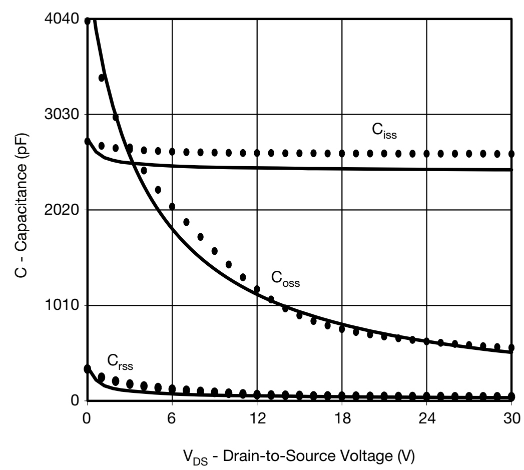
COMPARISON OF MODEL WITH MEASURED DATA T_J = 25 °C, unless otherwise noted

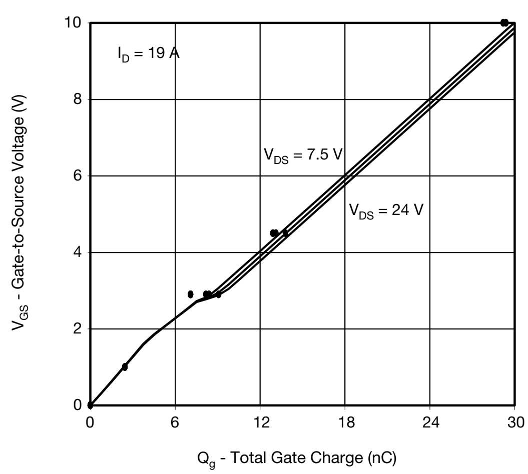
N-Channel 2

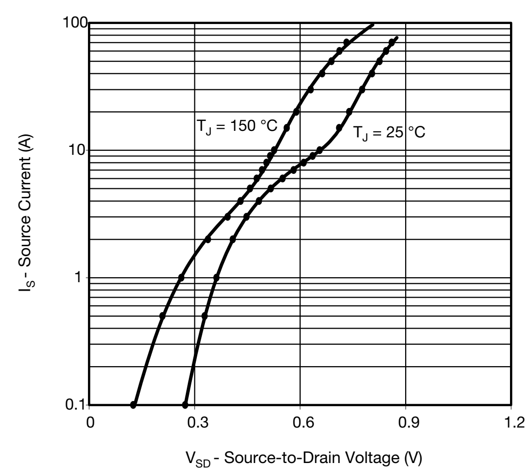












Note

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