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Vishay Siliconix

N-Channel 20 V (D-S) MOSFET

DESCRIPTION

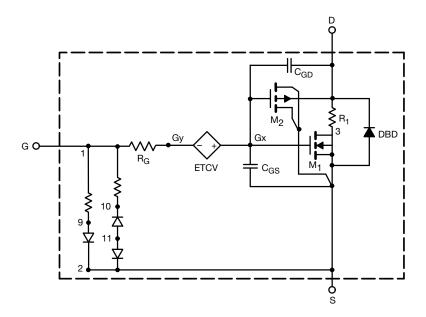
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model is extracted and optimized over the -55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$ temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Sub-circuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 °C to +125 °C Temperature Range
- · Model the Gate Charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.62	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 0.2 \text{ A}$	0.50	0.57	Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 0.1 \text{ A}$	0.59	0.67	
		$V_{GS} = 1.8 \text{ V}, I_D = 0.02 \text{ A}$	0.80	0.80	
		$V_{GS} = 1.5 \text{ V}, I_D = 0.01 \text{ A}$	0.90	0.90	
Forward Transconductance a	9 _{fs}	$V_{DS} = 10 \text{ V}, I_D = 0.2 \text{ A}$	1	1.2	S
Diode Forward Voltage	V _{SD}	I _S = 0.2 A	0.7	0.8	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	17	16	pF
Output Capacitance	Coss		7.4	7.5	
Reverse Transfer Capacitance	C _{rss}		3.4	3.5	
Total Gate Charge	Qg	$V_{DS} = 10 \text{ V}, V_{GS} = 8 \text{ V}, I_D = 0.2 \text{ A}$	0.29	0.52	nC
		$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 0.2 \text{ A}$	0.17	0.29	
Gate-Source Charge	Q _{gs}		0.03	0.03	
Gate-Drain Charge	Q_{gd}		0.03	0.03	

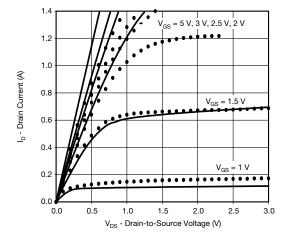
Notes

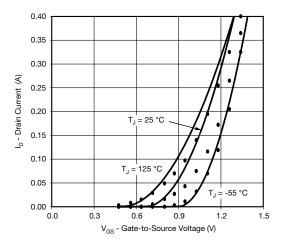
- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

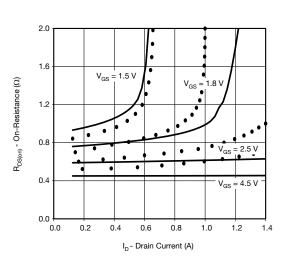
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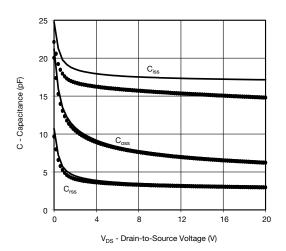
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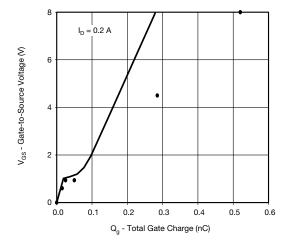
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25$ °C, unless otherwise noted)

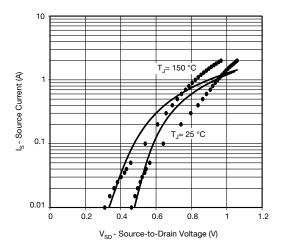












Note

Dots and squares represent measured data.
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Revision: 02-Oct-12 Document Number: 91000