Vishay Siliconix

N-Channel 25 V (D-S) MOSFET with Schottky Diode

DESCRIPTION

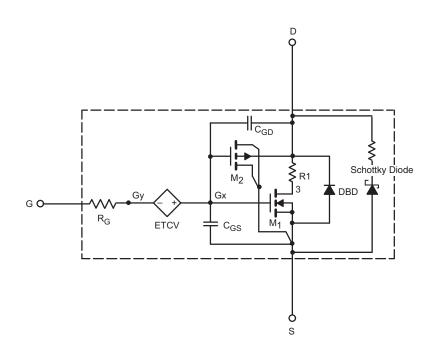
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to +125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

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A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- Model the gate charge



SUBCIRCUIT MODEL SCHEMATIC

Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.





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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.6	-	V
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 10 \text{ V}, I_D = 15 \text{ A}$	0.00082	0.00080	Ω
		V_{GS} = 4.5 V, I_D = 10 A	0.00120	0.00110	
Forward Transconductance ^a	g _{fs}	$V_{DS} = 5 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	120	67	S
Diode Forward Voltage	V _{SD}	I _S = 10 A	0.50	0.41	V
Dynamic ^b					
Input Capacitance	C _{iss}	V _{DS} = 5 V, V _{GS} = 0 V, f = 1 MHz	5070	5150	pF
Output Capacitance	Coss		2010	1950	
Reverse Transfer Capacitance	C _{rss}		348	350	
Total Gate Charge	Qg	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$	70	69	nC
		$V_{DS} = 5 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 10 \text{ A}$	33	31.5	
Gate-Source Charge	Q _{gs}		12.1	12.1	
Gate-Drain Charge	Q _{gd}		5.6	5.6	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

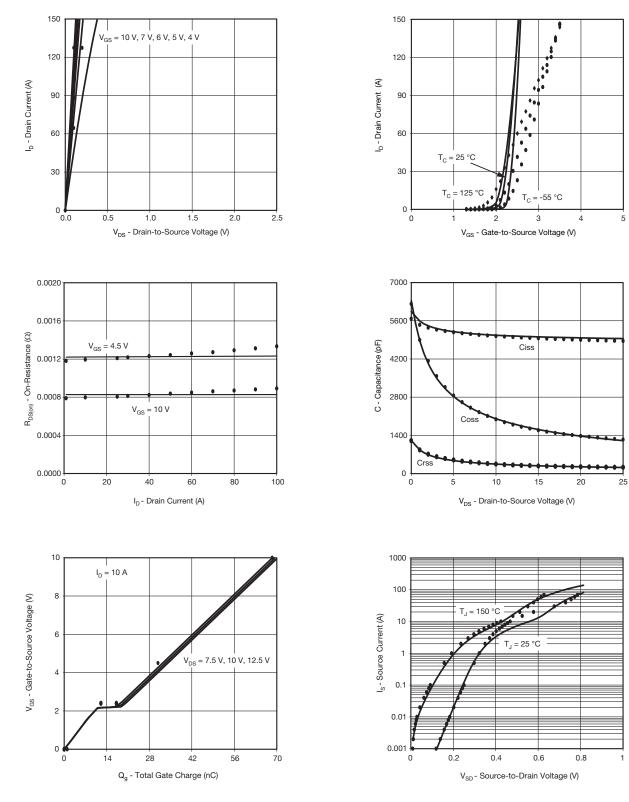
b. Guaranteed by design, not subject to production testing

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COMPARISON OF MODEL WITH MEASURED DATA (T_J = 25 °C, unless otherwise noted)



Note

• Dots and squares represent measured data. Copyright: Vishay Intertechnology, Inc.

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