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P-Channel 20 V (D-S) MOSFET

DESCRIPTION

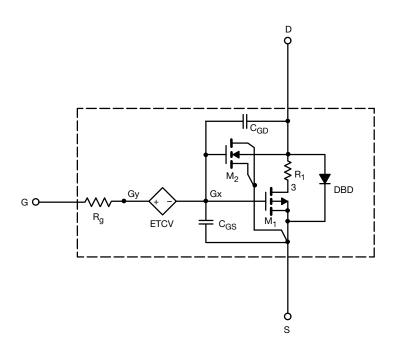
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-channel vertical DMOS
- · Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over -55 °C to 125 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



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SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu A$	0.70	-	V
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -3 \text{ A}$	0.015	0.017	Ω
		$V_{GS} = -2.5 \text{ V}, I_D = -3 \text{ A}$	0.020	0.020	
		$V_{GS} = -1.8 \text{ V}, I_D = -1 \text{ A}$	0.026	0.026	
Forward transconductance a	9 _{fs}	$V_{DS} = -5 \text{ V}, I_{D} = -3 \text{ A}$	21	22	S
Diode forward voltage	V _{SD}	I _S = -3 A	-0.70	-0.80	V
Dynamic ^b					
Input capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	3400	2500	pF
Output capacitance	C _{oss}		321	320	
Reverse transfer capacitance	C _{rss}		264	260	
Total gate charge	Q _g Q _{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_D = -3 \text{ A}$	42	54	nC
Total gate charge		V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -3 A	25	31.2	
Gate-source charge			3.9	2.7	
Gate-drain charge	Q _{gd}		5.3	6.3	

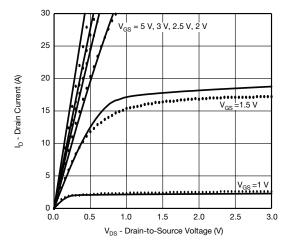
Notes

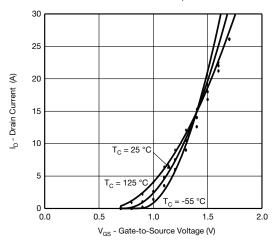
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing

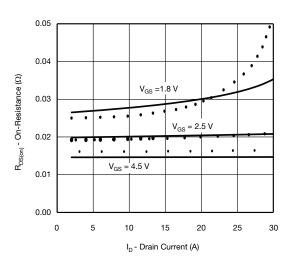
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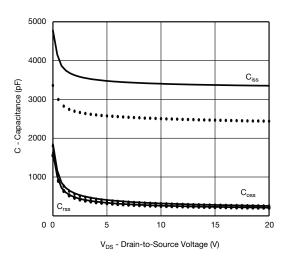
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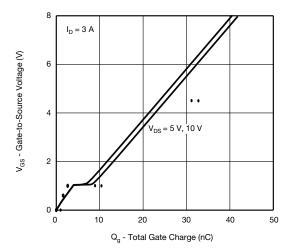
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25~^{\circ}C$, unless otherwise noted)

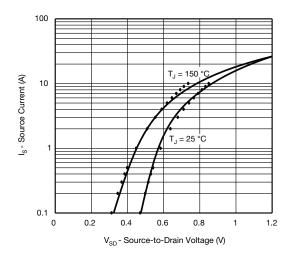












Note

 Dots and squares represent measured data Copyright: Vishay Intertechnology, Inc.



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