

Dual P-Channel 20 V (D-S) MOSFET

DESCRIPTION

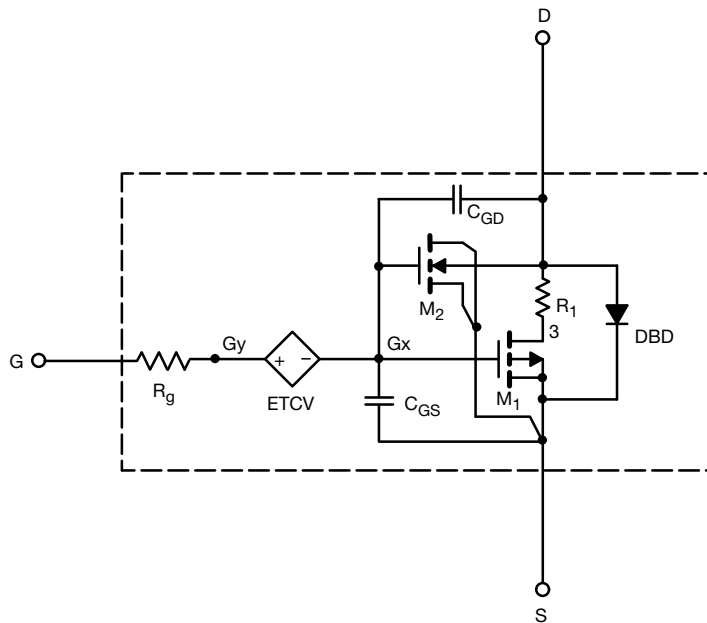
The attached SPICE model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to 125 °C temperature ranges under the pulsed 0 V to 5 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- P-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to 125 °C temperature range
- Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits



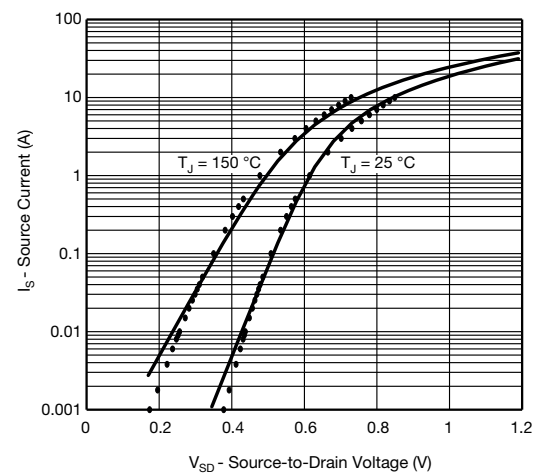
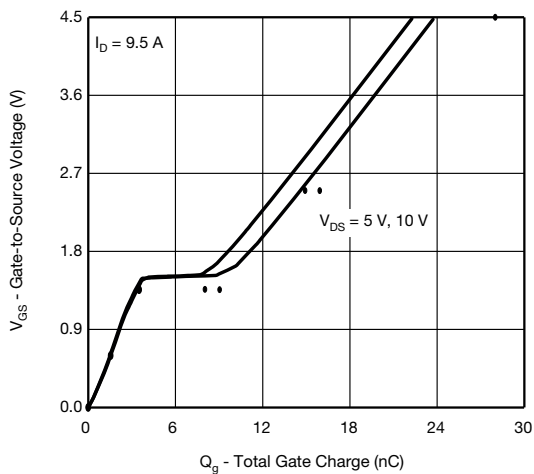
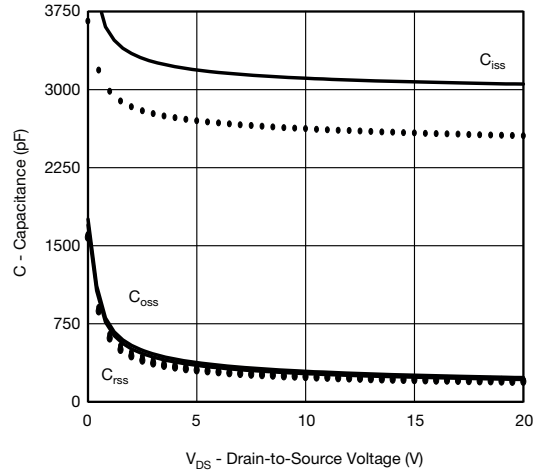
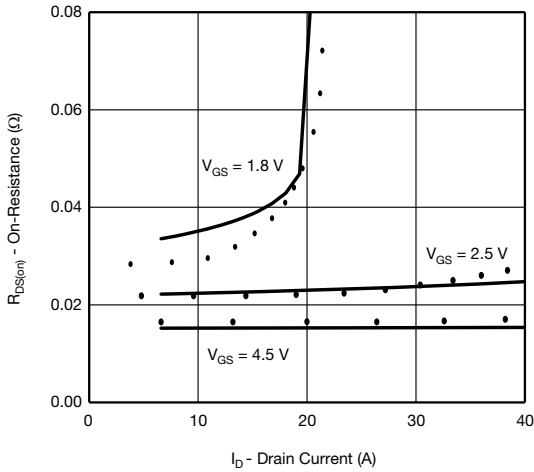
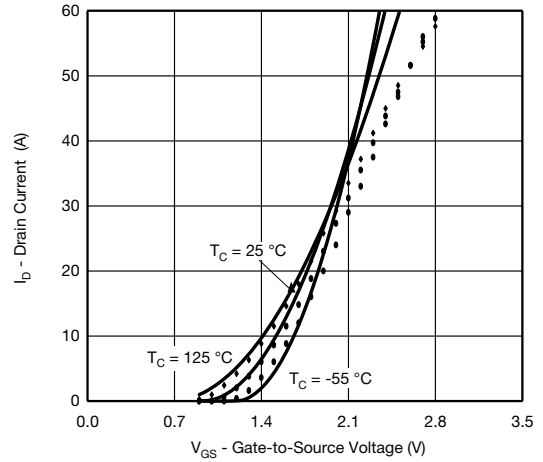
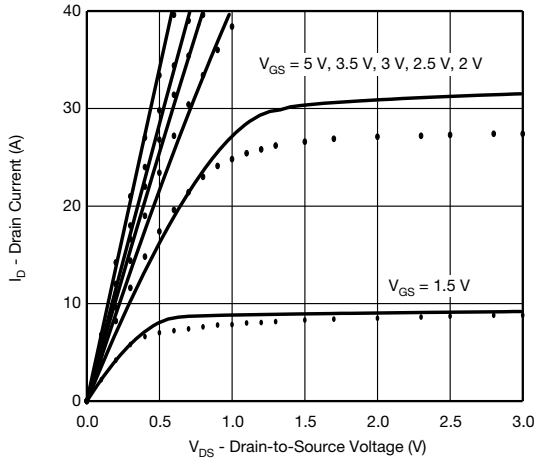
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	0.70	-	V
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = -4.5 V, I _D = -5 A	0.0160	0.0167	Ω
		V _{GS} = -2.5 V, I _D = -4 A	0.0221	0.0218	
		V _{GS} = -1.8 V, I _D = -2.5 A	0.0321	0.0285	
Forward transconductance ^a	g _{fs}	V _{DS} = -10 V, I _D = -5 A	32	32	S
Diode forward voltage	V _{SD}	I _S = -7.6 A	-0.80	-0.80	V
Dynamic ^b					
Input capacitance	C _{iss}	V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	3110	2565	pF
Output capacitance	C _{oss}		293	260	
Reverse transfer capacitance	C _{rss}		271	240	
Total gate charge	Q _g	V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -9.5 A	24	28	nC
Gate-source charge	Q _{gs}	V _{DS} = -10 V, V _{GS} = -2.5 V, I _D = -9.5 A	15	15.9	
Gate-drain charge	Q _{gd}		4	3.5	
			5	5.6	

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing



COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)



Note

- Dots and squares represent measured data

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