IGBT/MOSFET Gate Drive Optocoupler

INTRODUCTION TO IGBT

The Insulated Gate Bipolar transistor (IGBT) is a cross between a MOSFET (metal oxide semiconductor field effect transistor) and a BJT (bipolar junction transistor) since it combines the positive aspects of MOSFETs and BJTs.

The IGBT has the fast switching capability of the MOSFET and is capable of handling the high current values typical of a BJT. In addition, IGBTs have a lower on-state voltage drop and are capable of blocking higher voltages.

The IGBT, as a first approximation, can be modeled as a PNP transistor driven by a power MOSFET, as shown in figure 1.

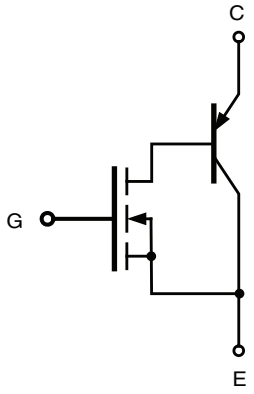

Fig. 1 - Simplified IGBT Equivalent Circuit

Figure 2 shows the most common symbols used for IGBT.

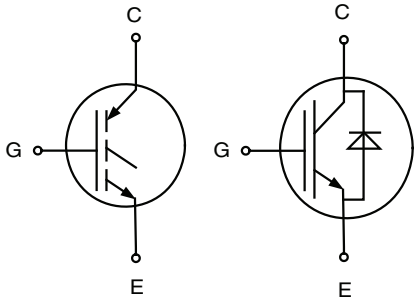

Fig. 2 - IGBT Symbols

The equivalent circuit for the input of IGBT is the same as a MOSFET and is purely capacitive. This allows the use of a voltage drive, which means that it is possible to have a less complex circuit with lower power consumption compared to a BJT. IGBTs are used for high current, high voltage applications when switching speed is important (table 1).

TABLE 1- IGBTs VS. MOSFETs

	IGBTs	POWER MOSFETs
TYPE	**VOLTAGE DRIVEN**	**VOLTAGE DRIVEN**
Current density per voltage drop	Very high, small trade-off with switching speed	High at low voltage low at high voltage
Switchung losses	Low to medium	Very low

IGBT SWITCHING BEHAVIOR

One of the important performance features of any switching device is the switching (turn-on and turn-off) characteristic, since significant power losses are incurred during these switching states.

When driving inductive loads, the device under goes higher stress. Hence, it makes sense to study the turn-on and turn-of time of the IGBT/MOSFET when driving inductive loads.

The IGBT's internal input capacitance (C_{GE}) and Miller capacitance (C_{GC}) impacts the IGBT turn-on behavior. But the C_{GC} effect is very small and negligible. Figure 3 illustrates the parasitic IGBT capacitances.

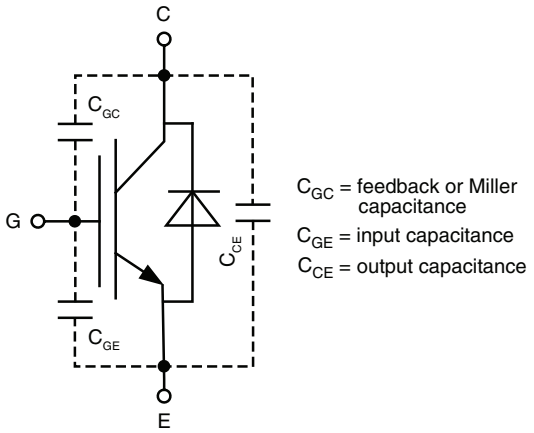

Fig. 3 - IGBT Parasitic Capacitances

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Most datasheets specify the voltage-dependent low-signal capacitance of IGBT/MOSFETs in the off-state (table 2).

TABLE 2 - IGBT AND MOSFET CAPACITANCE

CAPACITANCE	IGBTs	POWER MOSFETs
Input	$C_{iss} = C_{GE} + C_{GC}$	$C_{iss} = C_{GS} + C_{GD}$
Reverse transfer	$C_{rss} = C_{GC}$	$C_{rss} = C_{GD}$
Output	$C_{oss} = C_{GC} + C_{CE}$	$C_{oss} = C_{GD} + C_{DS}$

The turn-on behavior of the IGBT is identical to the power MOSFET, since the IGBT acts as a MOSFET during most of the turn-on interval. When a gate signal is applied, the gate emitter voltage of the IGBT rises from zero to $V_{GE(TH)}$, as shown in figure 4. This voltage rise is due to the gate resistance (R_{gate}) and the C_{GE}.

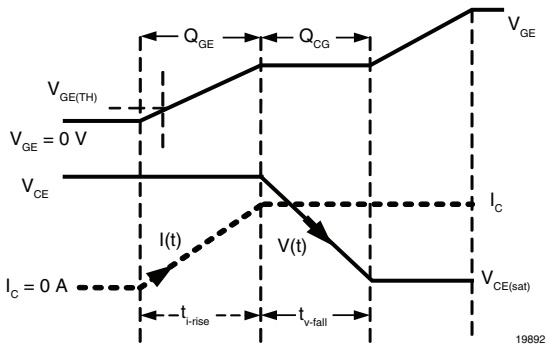

Fig. 4 - IGBT Turn-On Sequence

The turn-on time is a function of the output impedance of the drive circuit and the applied gate voltage. Hence, it is possible to control the turn-on speed of the device by choosing an appropriate value of gate resistance (R_{gate}).

In other words, by varying the R_{gate} it is possible to vary the time constant of the parasitic net equal to R_{gate} x (C_{GE}+C_{CG}) and then dV/dt. Therefore, the R_{gate} value strongly impacts the power losses, since its variation also affects the dV/dt slopes as illustrated in figure 5.

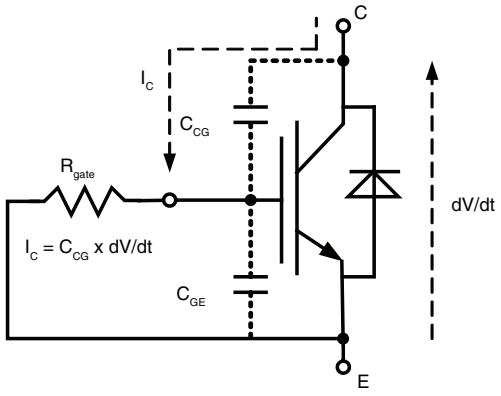

Fig. 5 - R_{gate} Effect on dV/dt

The turn-off behavior of the IGBT, as shown in figure 6, has a dual characteristic of both power MOSFET and BJT devices.

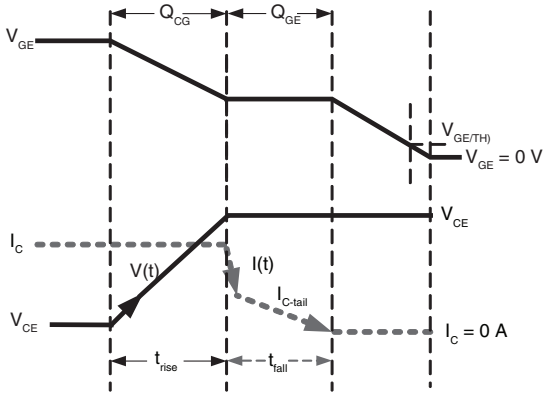

Fig. 6 - IGBT Turn-Off Sequence

At turn-off, the gate voltage begins to decrease until it reaches the value when the Miller effect occurs; during this time the V_{CE} voltage increases changing the output characteristics with constant I_C.

Next, the Miller effect and the V_{GE} voltage remain constant because of modulation of the collector gate capacitance, which is due to V_{CE} voltage rapidly increasing to its maximum value. During this time, the collector current begins to fall quickly, and continues with a “tail” which is due to recombination of minority carriers in the substrate.

The faster (and first) part of the I_C current is due to the turn-off of the MOSFET portion of the IGBT structure. The $I_{C\text{-}tail}$, which is due to the turn-off the BJT portion of the IGBT structure, causes the major part of the switching losses.

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IGBT POWER DISSIPATION

The maximum switching frequency of an IGBT is limited by its power dissipation during switching. The junction temperature (T_j) during normal operation depends on the amount of power dissipated from the device and the efficiency of the heat sink.

$$T_j = T_C + P_{tot} \times \theta_{JC} \quad (1)$$

To select a heat sink, which keeps the junction temperature at or below a given temperature, the following equation can be used:

$$\theta_{SA} = \frac{\Delta T}{P_{tot}} - \theta_{JC} - \theta_{CS} \quad (2)$$

Where:

θ_{SA} = heat sink to ambient thermal resistance
θ_{JC} = junction-to-case thermal resistance
θ_{CS} = case to heat sink thermal resistance
P_{tot} = total power dissipation
T_C = case temperature

When an efficient heat sink is used, T_C will be lowered. This means that the difference between junction-to-case temperature will be greater. Hence, a higher amount of power can be dissipated.

P_{tot} is the maximum continuous power dissipated by the device for a given case temperature. The maximum power dissipation is related to permissible case temperature rise and junction-to-case thermal resistance.

$$P_{tot} = \frac{T_J - T_C}{\theta_{JC}} \quad (3)$$

The main factor is to determine the P_{tot} of IGBT is the $V_{CE(SAT)}$ level, which is dependant on junction temperature, collector current ,and gate emitter voltage.

$$P_{tot} = I_{CE(ave)} \times V_{CE(sat)} \quad (4)$$

IGBT SWITCHING POWER LOSSES

When turning an IGBT on or off, the level of V_{GE} and R_{gate} affects the switching losses of the device. The effect of increasing V_{GE} or reducing R_{gate} is to reduce the delay time, rise time, and fall times of the device and hence to reduce the switching losses. Reducing the level of V_{GE} or increasing R_{gate} results in increased switching losses but can reduce electromagnetic interference (EMI). Other factors affecting the switching losses include the anti parallel diode (FWD), circuit inductance, snubbers, device junction temperature, operating voltage, and current. The use of FWD is illustrated in figure 7.

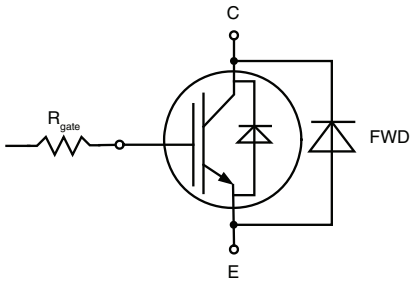

Fig. 7 - FWD is used with IGBT to Adjust Switching Speed

The reverse-recovery and turn-on characteristics of the FWD can be controlled to a certain extent by adjusting the speed of the IGBT. In the event of a diode becoming too snappy in an application, the IGBT turn-on can be slowed down, hence reducing the value of dV/dt applied to the diode and so reducing the diode losses. However, this is at the expense of increasing the IGBT losses. An alternative method of reducing the FWD losses in a bridge configuration is to turn on the IGBT with a reduced V_{GE}. This limits the peak reverse recovery current, I_{rr}, of the FWD in the opposite side of the arm, according to the IGBTs' forward output characteristic.

As illustrated in figures 4 and 6, there is a finite time interval, during both turn-on and turn-off of the IGBT, where finite V_{CE} and I_C coexist. C_{ISS}, C_{OSS}, and C_{RSS} affect the turn-on and turn-off times as well as turn-on and turn-off delay times and are responsible for some energy losses.

Average IGBT power losses during both turn-on and turn-off can be computed as follows:

$$E_{SW} = E_{SW(on)} + E_{SW(off)} \quad (5)$$

$$E_{SW} = \int V_{CE}(t) \times I_C(t)\, dt \quad (6)$$

$$E_{SW(on)} = \int^{i\text{-}rise} V_{CE} \times I_C(t) \times dt + \int^{v\text{-}fall} V_{CE}(t) \times I_C \times dt \quad (7)$$

$$E_{SW(on)} = \frac{1}{2} \times V_{CE} \times I_C \times (t_{i\text{-}rise} + t_{v\text{-}fall}) \quad (8)$$

$$E_{SW(off)} = \int^{v\text{-}rise} V_{CE}(t) \times I_C \times dt + \int^{i\text{-}fall} V_{CE} \times I_C(t) \times dt \quad (9)$$

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$$E_{SW(off)} = \frac{1}{2} \times V_{CE} \times (I_C \times t_{v\text{-}rise} + I_{C\text{-}tail} \times t_{i\text{-}fall}) \quad (10)$$

$$E_{SW} = \frac{1}{2} \times V_{CE} \times I_C \times (t_{on} + t_{off}) \quad (11)$$

Where:

E_{SW} = switching energy loss
t_{on} = $t_{i\text{-}rise}$ + $t_{v\text{-}fall}$ = turn-on time
t_{off} = $t_{v\text{-}rise}$ + $t_{i\text{-}fall}$ = turn-off time

$$P_{SW} = f_{SW} \times E_{SW} \quad (12)$$

Where:

P_{SW} = switching power loss
f_{SW} = switching frequency

Power dissipated during turn-on is calculated as follows:

$$P_{SW(on)} = \frac{1}{2} \times V_{CE} \times I_C \times f_{SW} \times t_{on} \quad (13)$$

Figure 6 indicates that the power dissipated during turn-off is due to two factors.

The first such factor is the speed at which the collector voltage reaches its maximum value. The second factor is the duration of the tail of the collector current. The collector tail current is due to the recombination of the minority carriers that cannot be extracted from the base of the PNP BJT section that is already open. The length of this “tail” depends on the lifetime of these carriers and causes the major part of the switching losses.

Hence, the turn-off power losses can be approximated as follows:

$$P_{SW(Off)} \approx \frac{1}{2} \times V_{CE} \times f_{SW} \times (I_C \times t_{v\text{-}rise} + I_{C\text{-}tail} \times t_{i\text{-}fall}) \quad (14)$$

The turn-off switching losses of the MOSFET portion of the IGBT structure are negligible. This is because the time that the MOSFET portion are responsible for the IGBT turn off is only a very small fraction of $t_{i\text{-}fall}$ time and much shorter time than that of the BJT portion.

IGBT GATE DRIVER IC POWER LOSSES

IGBTs are voltage controlled devices and require a gate voltage to establish collector emitter conduction. Due to the large input gate emitter capacitance (C_{GE}) of IGBTs, MOSFET drive techniques can be used where the off biasing needs to be stronger. The positive gate drive should be such that the full saturation is guaranteed and short-circuit current is limited. A negative voltage bias is used to improve the IGBT immunity to collector emitter dV/dt injected noise and to reduce turn-off losses. Figure 8 shows a simplified IGBT gate driver.

It is good practice to connect some back-to-back zener diodes directly across the gate emitter terminals of the IGBT. This prevents damage from over-voltage on the collector (by limiting the level of V_{GE}). This is because when a short circuit appears while the device is already conducting the voltage and collector current rise very quickly. The rapidly rising dV/dt coupled with the Miller capacitance (C_{GC}) can increase the effective V_{GE} seen by the IGBT, further increasing the short circuit current level.

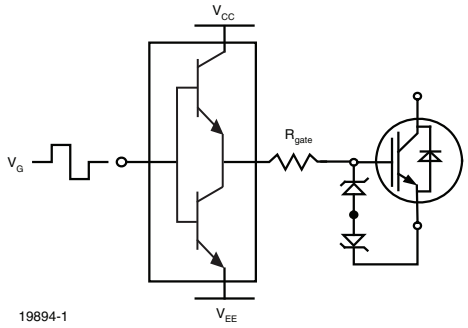

Fig. 8 - Simplified IGBT Gate Driver

The value of the gate resistance (R_{gate}) has a significant impact on the dynamic performance of the IGBTs. A smaller R_{gate} charges and discharges the IGBT input capacitance faster, which reduces the switching time and hence the switching losses and provides immunity to dV/dt turn on. But, a small R_{gate} can cause oscillation between the IGBT input capacitance and parasitic lead inductance.

The minimum peak current capability of the gate drive power source and the average power required to drive an IGBT is as follows:

$$I_{gate(peak)} = \pm \frac{\Delta V_{GE}}{R_{gate}} \quad (15)$$

Where:

$$\Delta V_{GE} = V_{GE(on)} + V_{GE(off)} \quad (16)$$

When determining the gate drive requirements for the switching IGBT, the key specification to look for is the gate charge. The main reason for looking at gate charge rather

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than gate capacitance is the Miller effect. The Miller capacitance (C_{GC}) effects on gate drive of IGBT are characterized in the gate charge value. Figure 3 is representative of parasitic gate capacitances.

The charging process for the gate of an IGBT is shown in figure 9.

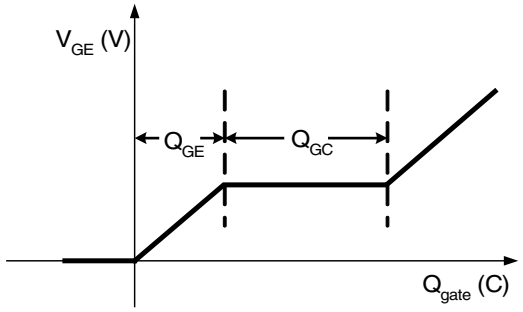

Fig. 9 - Total IGBT Gate Charge Waveform During Switching

First, the C_{GE} is charged (the C_{GC} is also being charged, but the amount of charge is very low and negligible). Once the C_{GE} is charged up to the gate threshold voltage ($V_{GE(TH)}$), the device begins to turn on and the current ramps up to the full value of current in the circuit. Once the full current is reached, the V_{CE} voltage begins to collapse and the gate voltage becomes flat due to C_{GC} being charged and the collector voltage falling off. After the collector voltage has fallen to its final level, the C_{GE} and C_{GC} are charged to the gate drive voltage.

To better understand gate charge, it can be shown with the following equations.

$$Q_{gate} = V_{GE} \times C_{gate} \quad (17)$$

$$C_{gate} = \frac{Q_{gate}}{V_{GE}} \quad (18)$$

Where:
Q_{gate} = total gate charge
C_{gate} = total gate capacitance
V_{GE} = driver's supply voltage

This means that the charging and discharging the IGBT gate can be seen as the charging and discharging a capacitor.

$$P_{gate} = \frac{1}{2} \times C_{gate} \times V_{GE}{}^{2} \times f_{SW} \quad (19)$$

Where:
f_{SW} = switching frequency

Hence, the power dissipated for the output of the IGBT driver IC is:

$$P_{Output} = C_{gate} \times V_{GE}{}^{2} \times f_{SW} \quad (20)$$

The amount of power dissipated in the IGBT driver IC emitter is:

$$P_{Emitter} = I_F \times V_F \times D \quad (21)$$

Where:
D = maximum LED duty cycle
I_F = LED forward current
V_F = LED forward voltage

The amount of power dissipated in the IGBT driver internal circuitry is:

$$P_{Internal} = I_{CC} \times (V_{CC} - V_{EE}) \quad (22)$$

Where:
I_{CC} = Supply current, output open

The total gate driver IC power losses are:

$$P_{gate-driver(tot)} = P_{Output} + P_{Emitter} + P_{Internal} \quad (23)$$

In many applications, the gate drive circuitry needs to be isolated from the control circuit to provide level shifting and improve noise immunity and safety. This is what the Vishay IGBT driver provides by means of optical isolation.

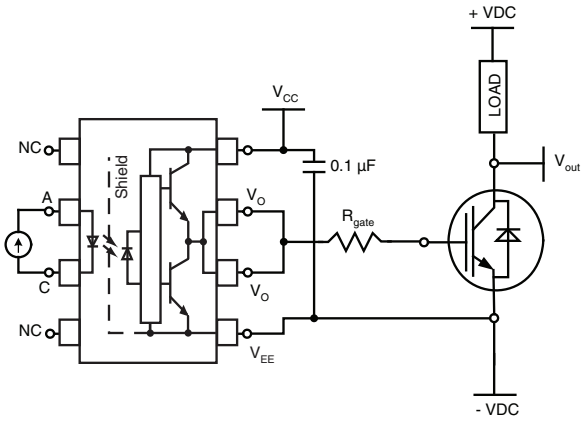

Fig. 10 - Simplified Vishay IGBT Driver Circuit

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IGBT GATE DRIVE REQUIREMENTS AND FEATURES

Minimum Output Current

A very important requirement for an IGBT gate driver optocoupler is to supply the minimum output or gate current (I_{OL} or I_{gate}) to switch the IGBT to the low impedance state. This is illustrated in figure 11.

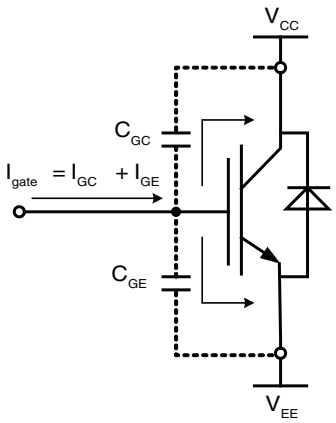

Fig. 11 - IGBT Gate Current

The I_{OL} is specified when output voltage is low, i.e. when the gate drive optocoupler is charging the IGBT gate.
Hence, the load draws the highest output current. The required I_{OL} or I_{gate} to switch the IGBT can be calculated by using the gate capacitances of the IGBT.

$$V_{GE/GC} = \frac{1}{C_{GE/GC}} \times \int I_{GE/GC}(t)dt \quad (24)$$

$$V_{GE/GC} = \frac{1}{C_{GE/GC}} \times I_{GE/GC} \times t_{SW} \quad (25)$$

$$I_{GE/GC} = \frac{V_{GE/GC} \times C_{GE/GC}}{t_{SW}} \quad (26)$$

For $$I_{gate} = I_{GE} + I_{GC} \quad (27)$$

$$I_{gate} = \frac{V_{GE} \times C_{GE}}{t_{SW}} + \frac{V_{GC} \times C_{GC}}{t_{SW}} \quad (28)$$

Where:
t_{SW} = switching time
I_{GE} = current in to C_{GE}
I_{GC} = current in to C_{GC}

Gate Resistor (R_{gate}) Value

R_{gate} will need to be selected such that the maximum peak output current rating of the gate driver optocoupler ($I_{OL(peak)}$) is not exceeded.

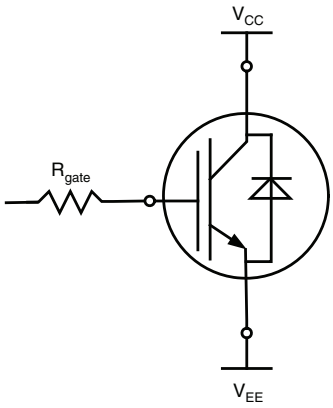

Fig. 12 - IGBT Gate Resistor (R_{gate})

The following equation can be used to calculate the appropriate R_{gate} value:

$$R_{gate} = \frac{V_{CC} - V_{EE} - V_{OL}}{I_{OL(peack)}} \quad (29)$$

Where:
V_{OL} = low-level output voltage of the gate driver optocoupler

UVLO

The minimum acceptable gate drive voltage for an IGBT is important because falling below this value will result in switching from on state to a highly dissipative linear mode. Hence, the Vishay IGBT drivers have under-voltage lock-out (UVLO) to ensure that gate drive is removed for low drive condition. This will prevent the IGBT from entering the linear conductive mode.

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LED DRIVE CONSIDERATIONS

As shown in figure 13, Vishay IGBT/MOSFET driver IC has a transparent faraday shield on the driver IC, represented by the dashed line between the emitter (input LED) and detector.

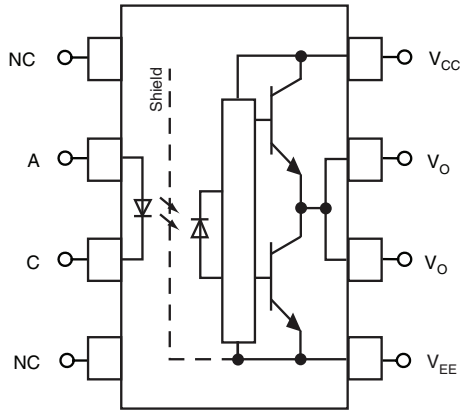

Fig. 13 - Vishay IGBT Driver

This shield diverts the capacitively coupled current away from the sensitive IC circuitry. Although the shield improves common mode transient response (CMTR) performance, it does not eliminate the capacitive coupling between the LED and V_{CC} and V_{EE} output pins. These capacitances are shown in figure 14.

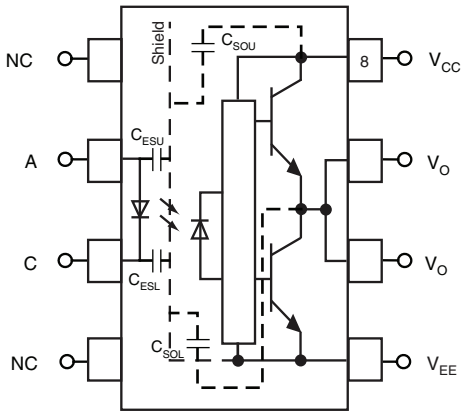

Fig. 14 - IGBT Driver Parasitic Capacitance

This capacitive coupling causes perturbations in the LED current during common-mode transients and becomes the major source of CMTR failures for a shielded optocoupler. The main design objective of a high-CMTR LED drive circuit becomes keeping the LED in the proper state (on or off) during common-mode transients.

The following methods can be used to ensure the LED is in the desired (on or off) state.

LED On-State (CM_H)

A high-CMTR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient.

LED Off-State (CM_L)

A high-CMTR LED drive circuit needs to keep the LED off ($V_F < V_{F(OFF)}$) during common mode transients. As long as the low-state voltage developed across the logic gate (driving the LED) is less than $V_{F(OFF)}$, the LED will remain off and no common-mode failure will occur. The circuit shown in figure 15 is recommended for high-CMTR performance.

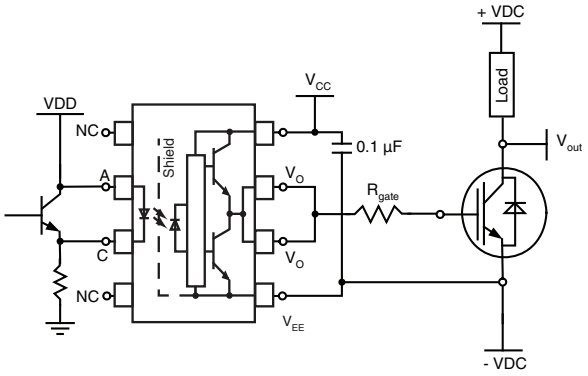

Fig. 15 - Recommended LED Drive Circuit for High CMTR Performance

IGBT/MOSFET DRIVER DESIGN CONSIDERATIONS

When designing and building driver circuits for an IGBT/MOSFET, the following will need to be taken in to consideration to prevent unwanted voltage spikes, oscillation or ringing, and false turn-on.

1. Layout
2. Power supply by-passing
3. Mismatch of driver to the driven IGBT/MOSFET

To ensure a robust and problem free IGBT/MOSFET driver, designers are advised to pay close attention to what is recommended in the next few paragraphs.

Layout

A very crucial point is proper grounding. A very low-impedance path for current return to ground avoiding loops is a good design practice. The three paths for returning current to ground are between:

1. Driver and the logic driving it
2. Driver and its own power supply
3. Driver and the source/emitter of the IGBT being driven

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All these paths should be very short in length to reduce inductance. Also, these paths should be as wide as possible to reduce resistance. In addition, these ground paths need to be kept separate to avoid returning ground current from the load to affect the logic line. It is very important to note that all ground points in the circuit should return to the same physical point to avoid generating differential ground potentials.

Power Supply By-Passing

Since turning an IGBT/MOSFET on and off amounts to charging and discharging large capacitive loads, the peak charge current need to be within the capability of drive circuit. At the same time the driver will have to draw this current from its power supply in a short period of time. This means that using of proper by-pass capacitors for the power supply becomes very important. A pair of by-pass capacitors of at least 10 times the load capacitance with complementary impedance, used in parallel and very close to the V_{CC} pin, can take care of this issue. These by-pass capacitors should have the lowest possible equivalent series resistance (ESR) and equivalent series inductance (ESL) and the capacitor lead lengths should be as short as possible.

Mismatch of Driver to the Driven IGBT/MOSFET

Since all IGBT/MOSFET driver ICs have some losses, it is necessary to calculate the power dissipated in the driver for a worst-case condition. The total power dissipated in the IGBT driver IC (as described previously) is:

$$P_{gate-driver(tot)} = P_{Output} + P_{Emitter} + P_{Internal} \quad (23)$$

Where:

$$P_{Output} = C_{gate} \times V_{GE}{}^2 \times f_{SW} \quad (20)$$

$$P_{Emitter} = I_F \times V_F \times D \quad (21)$$

$$P_{Internal} = I_{CC} \times (V_{CC} - V_{EE}) \quad (22)$$

Since ambient temperature in the vicinity of the IGBT/MOSFET driver will have an effect on the actual power dissipation capability of the driver, the maximum allowable power dissipation at this temperature will need to be derated accordingly (in comparison to room temperature). The selected IGBT/MOSFET driver can only be used if the maximum allowable power dissipation at this temperature is within the capability of this IGBT/MOSFET driver.

VISHAY IGBT DRIVER APPLICATION EXAMPLES

Some applications for the IGBT/MOSFET drivers are:

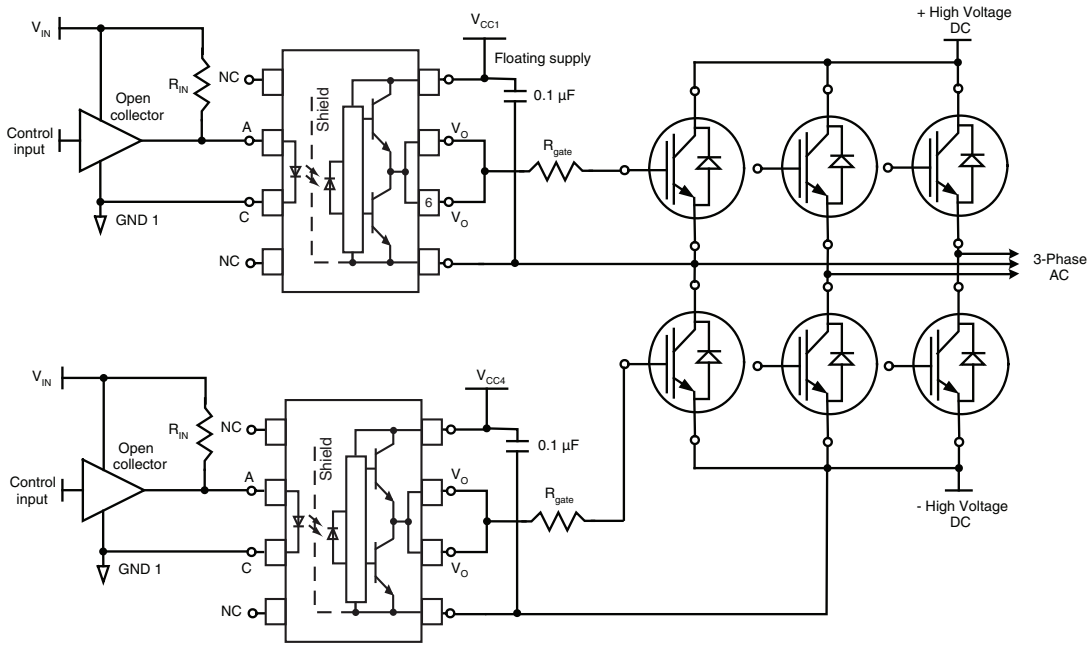

Fig. 16 - 3-Phase Motor Drive Application

Note

- The value for R_{IN} is dependent upon V_{IN}, the desired LED input current (I_F), and input forward voltage (V_F).

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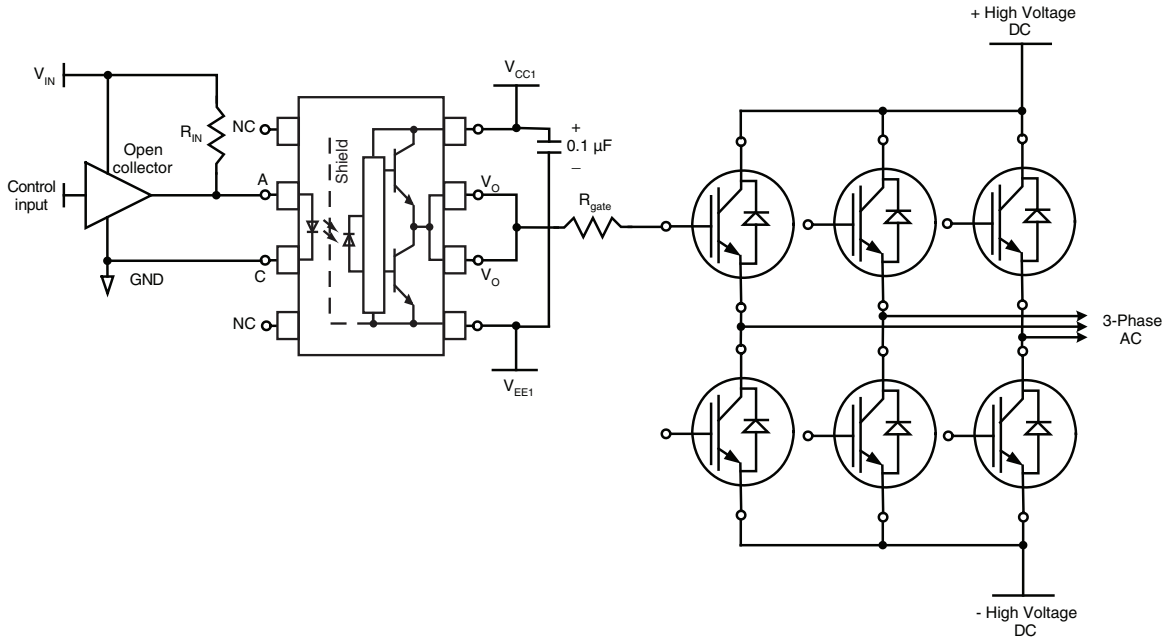

Fig. 17 - Negative IGBT Gate Drive Application

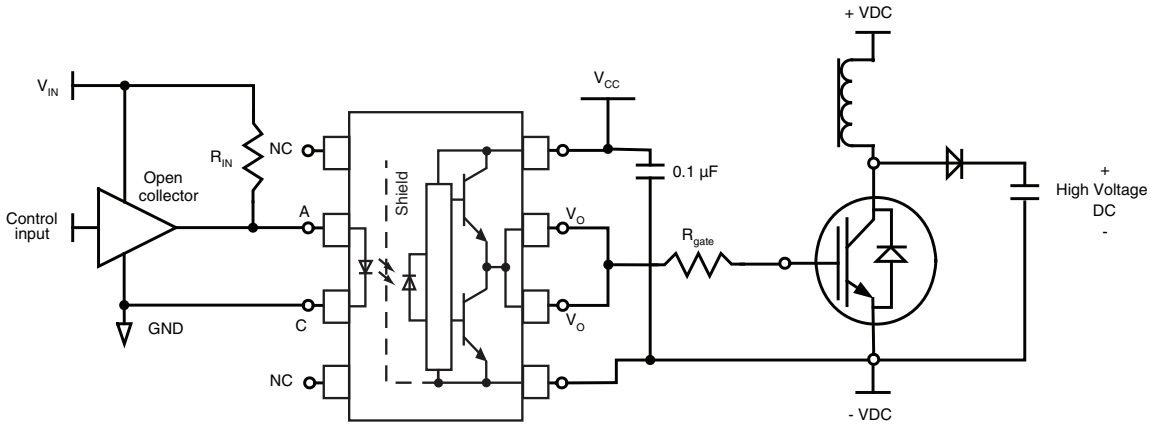

Fig. 18 - Boost Converter Application

APPLICATION NOTE