RoHS

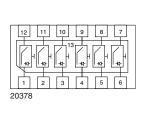
HALOGEN FREE

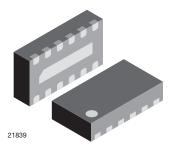
**GREEN** 



## Vishay Semiconductors

## 6-Channel EMI-Filter with ESD-Protection





#### **FEATURES**

- Ultra compact LLP2513-13L package
- Low package profile of 0.6 mm
- 6-channel EMI-filter
- · Low leakage current
- Line resistance  $R_S = 100 \Omega$
- Typical cut off frequency f<sub>3dB</sub> = 240 MHz
- ESD-protection acc. IEC 61000-4-2 ± 10 kV contact discharge
  - ± 12 kV air discharge
- e4 precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- Material categorization: for definitions of compliance please see <a href="https://www.vishay.com/doc?99912"><u>www.vishay.com/doc?99912</u></a>

# MARKING (example only)

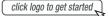


Dot = pin 1 marking

YY = type code (see table below)

XX = date code

### **DESIGN SUPPORT TOOLS**





ORDERING INFORMATION					
DEVICE NAME	CE NAME ORDERING CODE		MINIMUM ORDER QUANTITY		
VEMI65AC-HCI	VEMI65AC-HCI-GS08	3000	15 000		

PACKAGE DATA						
DEVICE NAME	PACKAGE NAME	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VEMI65AC-HCI	LLP2513-13L	9T	5.5 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

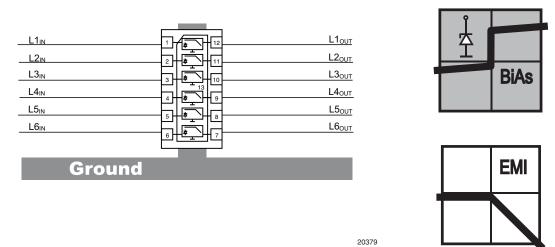
ABSOLUTE MAXIMUM RATINGS						
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT		
Peak pulse current	All I/O pin to pin 13; acc. IEC 61000-4-5; $t_p = 8/20 \mu s$ ; single shot	I <sub>PPM</sub>	2	А		
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V	± 10	kV		
	Air discharge acc. IEC 61000-4-2; 10 pulses	$V_{ESD}$	± 12			
Operating temperature	Junction temperature	TJ	-40 to +125	°C		
Storage temperature		T <sub>STG</sub>	-55 to +150	°C		



## Vishay Semiconductors

### **APPLICATION NOTE**

With the VEMI65AC-HCI 6 different signal or data lines can be filtered and clamped to ground. Due to the different clamping levels in forward and reverse direction the clamping behaviour is <u>Bi</u>directional and <u>Asymmetric</u> (BiAs).



The 6 independent EMI-filter are placed between

pin 1 and pin 12,

pin 2 and pin 11,

pin 3 and pin 10,

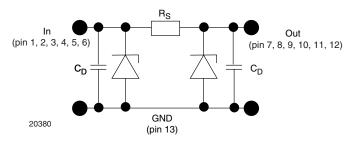
pin 4 and pin 9,

pin 5 and pin 8 and

pin 6 and pin 7.

They all are connected to a common ground pin 13 on the backside of the package.

The circuit diagram of one EMI-filter-channel shows two identical Z-diodes at the input to ground and the output to ground. These Z-diodes are characterized by the breakthrough voltage level ( $V_{BR}$ ) and the diode capacitance ( $C_D$ ). Below the breakthrough voltage level the Z-diodes can be considered as capacitors. Together with these capacitors and the line resistance  $R_S$  between input and output the device works as a low pass filter. Low frequency signals ( $f < f_{3dB}$ ) pass the filter while high frequency signals ( $f > f_{3dB}$ ) will be shorted to ground through the diode capacitances  $C_D$ .



Each filter is symmetrical so that both ports can be used as input or output.



# Vishay Semiconductors

PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of channels which can be protected	N <sub>channel</sub>	-	-	6	channel
Reverse stand off voltage	Max. reverse working voltage	V <sub>RWM</sub>	-	-	5	V
Reverse voltage	at I <sub>R</sub> = 1 μA	V <sub>R</sub>	5	-	-	V
Reverse current	at V <sub>R</sub> = V <sub>RWM</sub>	I <sub>R</sub>	-	< 0.1	1	μA
Reverse break down voltage	at I <sub>R</sub> = 1 mA	$V_{BR}$	6	-	-	V
Pos. clamping voltage	at I <sub>PP</sub> = 1 A applied at the input, measured at the output; acc. IEC 61000-4-5	V <sub>C-out</sub>	=	-	7	V
	at I <sub>PP</sub> = I <sub>PPM</sub> = 2 A applied at the input, measured at the output; acc. IEC 61000-4-5	V <sub>C-out</sub>	-	-	8	V
Neg. clamping voltage	at I <sub>PP</sub> = - 1 A applied at the input, measured at the output; acc. IEC 61000-4-5	V <sub>C-out</sub>	-1	-	-	V
	at I <sub>PP</sub> = I <sub>PPM</sub> = - 2 A applied at the input, measured at the output; acc. IEC 61000-4-5	V <sub>C-out</sub>	-1.2	-	-	V
Input capacitance	at $V_R = 0 V$ ; $f = 1 MHz$	C <sub>IN</sub>	-	20	-	pF
	at V <sub>R</sub> = 2.5 V; f = 1 MHz	C <sub>IN</sub>	-	13	-	pF
ESD-clamping voltage	at ± 10 kV ESD-pulse acc. IEC 61000-4-2	V <sub>CESD</sub>	-	7.5	-	V
Line resistance	Measured between input and output; $I_S = 10 \text{ mA}$	R <sub>S</sub>	90	100	110	Ω
Cut-off frequency	$V_{IN} = 0 \text{ V}$ ; measured in a 50 $\Omega$ system	f <sub>3dB</sub>	-	240	-	MHz

### TYPICAL CHARACTERISTICS (T<sub>amb</sub> = 25 °C, unless otherwise specified)

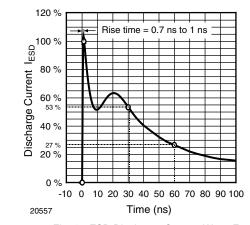


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega/150$  pF)

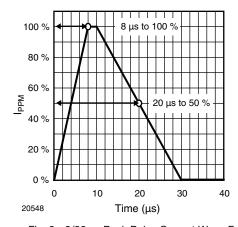


Fig. 2 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5





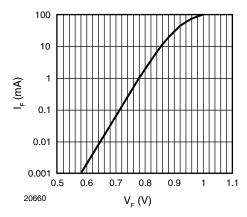


Fig. 3 - Typical Forward Current  $I_F$  vs. Forward Voltage  $V_F$ 

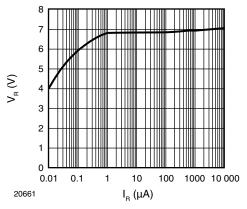


Fig. 4 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$ 

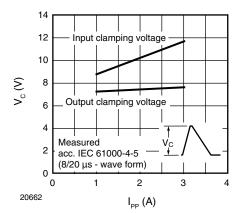


Fig. 5 - Typical Peak Clamping Voltage  $V_{C}$  vs. Peak Pulse Current  $I_{PP}$ 

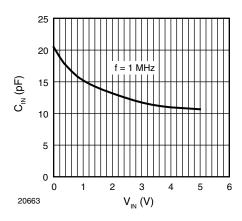


Fig. 6 - Typical Input Capacitance  $C_{\text{IN}}$  vs. Input Voltage  $V_{\text{IN}}$ 

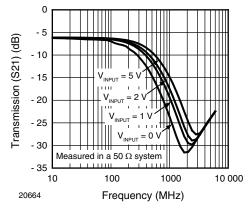
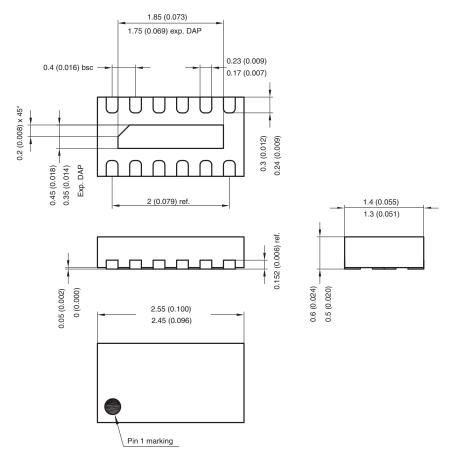


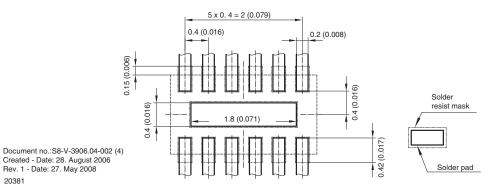
Fig. 7 - Typical Small Signal Transmission (S21) at  $Z_{O}$  = 50  $\Omega$ 

# Vishay Semiconductors

### PACKAGE DIMENSIONS in millimeters (inches): LLP2513-13L



#### Foot print recommendation:





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