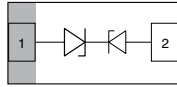
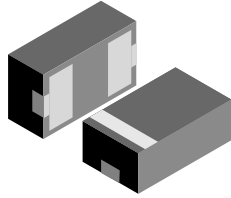




## Bidirectional Asymmetrical (BiAs) Single Line ESD Protection Diode in LLP1006-2L



20950



20855

### MARKING (example only)



21121

Bar = pin 1 marking  
Y = type code (see table below)  
X = date code

### DESIGN SUPPORT TOOLS click logo to get started



### FEATURES

- Ultra compact LLP1006-2L
- Low package height < 0.4 mm
- 1-line ESD protection
- Working range -7 V up to +14 V or -14 V up to +7 V
- Low leakage current < 0.1  $\mu$ A
- Low load capacitance typical  $C_D = 8$  pF
- ESD immunity acc. IEC 61000-4-2  
± 25 kV contact discharge  
± 30 kV air discharge
- e4 - precious metal (e.g. Ag, Au, NiPd, NiPdAu) (no Sn)
- e3 - Sn  
Tin plated exposed side wall of leadframe.  
Soldering can be checked by standard vision inspection.  
(AOI = Automated Outgoing Inspection)  
No X-ray necessary
- PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION				
PIN PLATING	DEVICE NAME	ORDERING CODE	TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL)	MINIMUM ORDER QUANTITY
e4	VCUT0714A-HD1	VCUT0714A-HD1-GS08	8000	8000
e3	VCUT0714AHD1	VCUT0714AHD1-G3-08	10 000	100 000

PACKAGE DATA							
DEVICE NAME	PACKAGE NAME	PIN PLATING	TYPE CODE	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
VCUT0714A-HD1	LLP1006-2L	e4	B	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals
VCUT0714AHD1	LLP1006-2L	e3	7	0.72 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

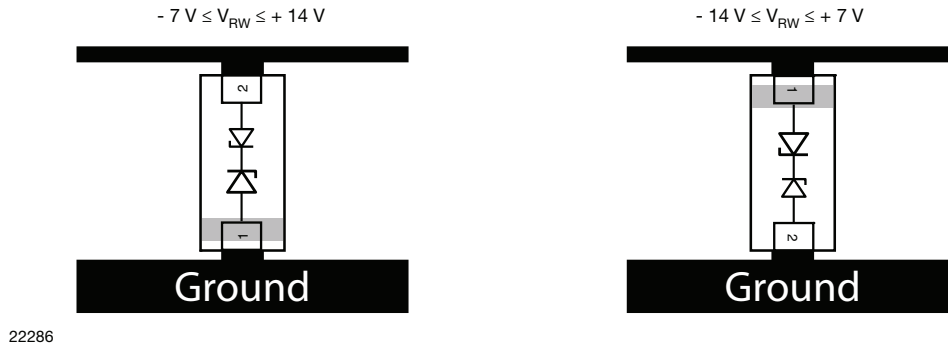
ABSOLUTE MAXIMUM RATINGS VCUT0714A-HD1				
PARAMETER	TEST CONDITIONS	SYMBOL	VALUE	UNIT
Peak pulse current	Pin 1 to pin 2 acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot	I <sub>PPM</sub>	5	A
	Pin 2 to pin 1 acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot		2	A
Peak pulse power	Pin 1 to pin 2 acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot	P <sub>PP</sub>	63	W
	Pin 2 to pin 1 acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot		54	W
ESD immunity	Contact discharge acc. IEC 61000-4-2; 10 pulses	V <sub>ESD</sub>	± 25	kV
	Air discharge acc. IEC 61000-4-2; 10 pulses		± 30	kV
Operating temperature	Junction temperature	T <sub>J</sub>	-40 to +125	°C
Storage temperature		T <sub>STG</sub>	-55 to +150	°C

PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)

This Vishay product is protected by one or more United States and international patents.

## CUT THE SPIKES WITH VCUT0714A-HD1

The VCUT0714A-HD1 is a bidirectional but asymmetrical (BiAs) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VCUT0714A-HD1 offers a high isolation (low leakage current, small capacitance) within the specified working range of -7 V to +14 V or -14 V and +7 V. Due to the short leads and small package size of the tiny LLP1006-2L package the line inductance is very low, so that fast transients like an ESD strike can be clamped with minimal over- or undershoots.



<b>ELECTRICAL CHARACTERISTICS VCUT0714A-HD1</b> (pin 2 to pin 1) ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	14	V
Reverse voltage	At $I_R = 0.1\text{ }\mu\text{A}$	$V_R$	14	-	-	V
Reverse current	At $V_{RWM} = 14\text{ V}$	$I_R$	-	-	0.1	$\mu\text{A}$
Reverse breakdown voltage	At $I_R = 1\text{ mA}$	$V_{BR}$	14.5	-	-	V
Reverse clamping voltage	At $I_{PP} = 1\text{ A}$	$V_C$	-	-	27	V
	At $I_{PP} = I_{PPM} = 2\text{ A}$	$V_C$	-	-	30	V
Capacitance	At $V_R = 0\text{ V}$ ; $f = 1\text{ MHz}$	$C_D$	-	8	8.5	pF
	At $V_R = 7\text{ V}$ ; $f = 1\text{ MHz}$	$C_D$	-	4	-	pF

<b>ELECTRICAL CHARACTERISTICS</b> (pin 1 to pin 2) ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)						
PARAMETER	TEST CONDITIONS/REMARKS	SYMBOL	MIN.	TYP.	MAX.	UNIT
Protection paths	Number of lines which can be protected	$N_{channel}$	-	-	1	lines
Reverse stand-off voltage	Max. reverse working voltage	$V_{RWM}$	-	-	7	V
Reverse voltage	At $I_R = 0.1\text{ }\mu\text{A}$	$V_R$	7	-	-	V
Reverse current	At $V_{RWM} = 7\text{ V}$	$I_R$	-	-	0.1	$\mu\text{A}$
Reverse breakdown voltage	At $I_R = 1\text{ mA}$	$V_{BR}$	7.3	-	-	V
Reverse clamping voltage	At $I_{PP} = 1\text{ A}$	$V_C$	-	-	13	V
	At $I_{PP} = I_{PPM} = 5\text{ A}$	$V_C$	-	-	17	V
Capacitance	At $V = 0\text{ V}$ ; $f = 1\text{ MHz}$	$C_D$	-	8	8.5	pF
	At $V = 3.5\text{ V}$ ; $f = 1\text{ MHz}$	$C_D$	-	6.4	-	pF

**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified)

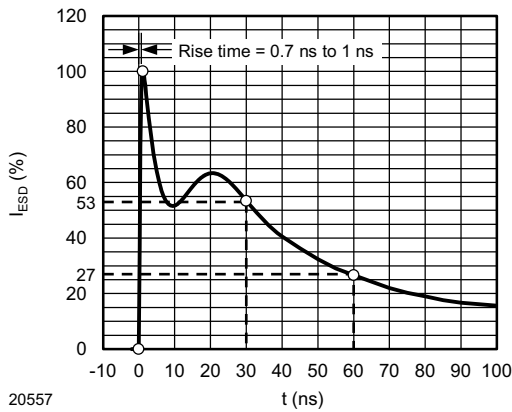


Fig. 1 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

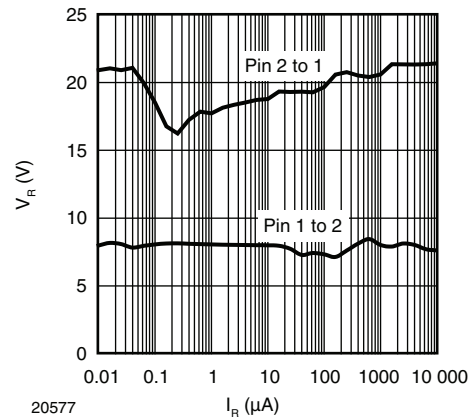


Fig. 4 - Typical Reverse Voltage  $V_R$  vs. Reverse Current  $I_R$

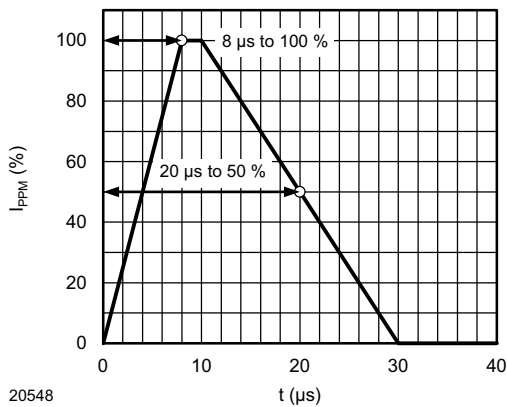


Fig. 2 - 8/20  $\mu\text{s}$  Peak Pulse Current Wave Form acc. IEC 61000-4-5

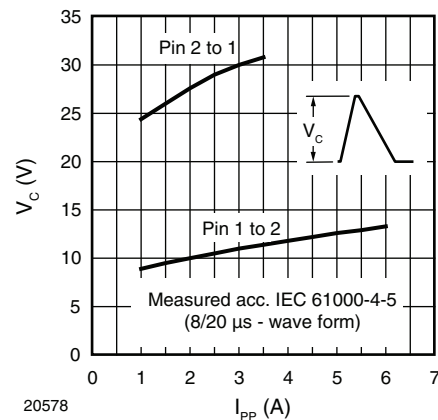


Fig. 5 - Typical Peak Clamping Voltage  $V_C$  vs. Peak Pulse Current  $I_{PP}$

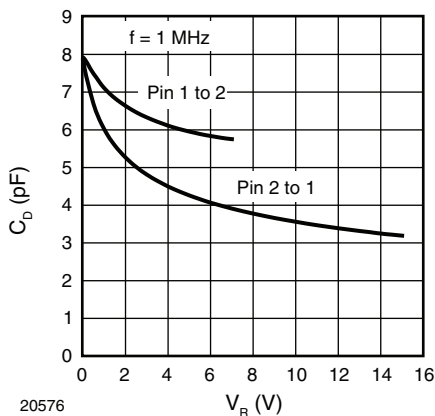


Fig. 3 - Typical Capacitance  $C_D$  vs. Reverse Voltage  $V_R$

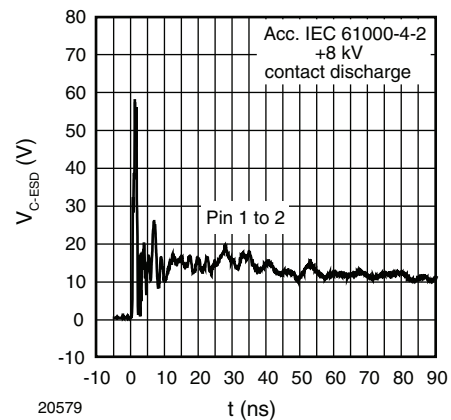


Fig. 6 - Typical Clamping Performance at +8 kV Contact Discharge (acc. IEC 61000-4-2)

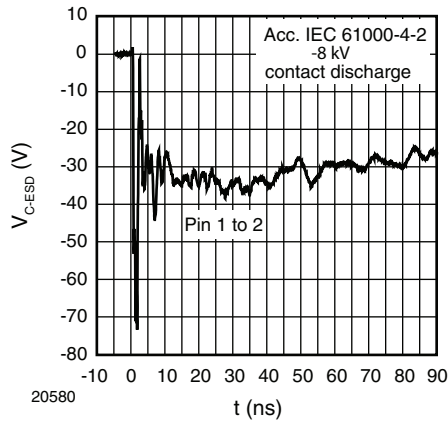


Fig. 7 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

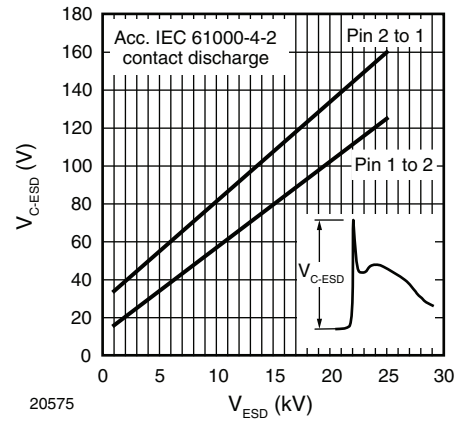
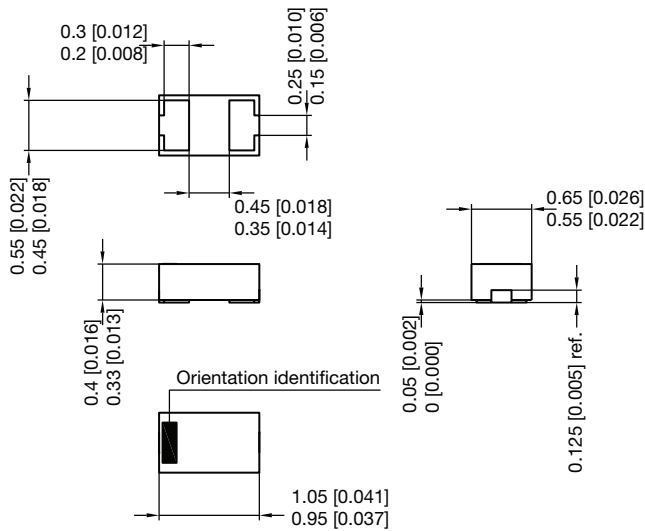
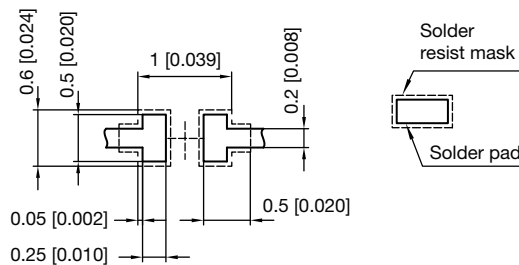


Fig. 8 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

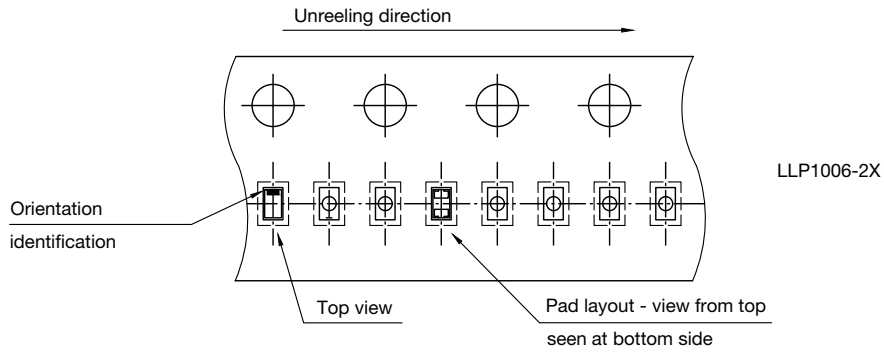
## PACKAGE DIMENSIONS in millimeters (inches): LLP1006-2L



Foot print recommendation:



Pad Design Patented:  
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S8-V-3906.04-017 (4)  
02.05.2017  
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