VISHAY SEMICONDUCTORS’ CONTINUOUS IMPROVEMENT

- Quality training for ALL personnel including production, development, marketing and sales departments
- Zero defect mindset
- Permanent quality improvement process
- Total Quality Management (TQM)
- Vishay Semiconductors’ Quality Policy established by the management board
- Quality system certified per ISO 9001:2008
- Quality system certified per ISO/TS 16949:2009
- Environmental system certified per ISO 14001:2004

VISHAY SEMICONDUCTORS’ TOOLS FOR CONTINUOUS IMPROVEMENT

- Vishay Semiconductors follows the rules of the EFQM - Quality - Management system
- Vishay Semiconductors qualifies materials, processes and process changes
- Vishay Semiconductors uses process FMEA (failure mode and effects analysis) for all processes. Process and machine capability as well as Gauge R & R (Repeatability & Reproducibility) are proven
- Vishay Semiconductors’ internal qualifications correspond to IEC 68-2 and MIL-STD 883 and AEC-Q101
- Vishay Semiconductors periodically requalifies device types (long term monitoring)
- Vishay Semiconductors uses SPC for significant production parameters. SPC is performed by trained operators
- Vishay Semiconductors’ 2 x 100 % testing of final products
- Vishay Semiconductors’ lot release is carried out via sampling. Sampling acceptance criterion is always c = 0
CREATE FIRST-CLASS QUALITY, ON-TIME DELIVERY, AND SATISFY CUSTOMERS’ REQUIREMENTS

Fig. 2 - Vishay Semiconductor, A-Voecklabruck, ISO 9001:2008

Fig. 3 - Vishay Semiconductor, A-Voecklabruck, ISO/TS 16949:2009

Fig. 4 - Vishay Semiconductor, A-Voecklabruck, ISO 14001

Fig. 5 - Vishay Semiconductor, D-Heilbronn, ISO 9001:2000
GENERAL QUALITY FLOW CHART

Development

Material

Incoming inspection

Qualification

Production

Wafer processing

Quality control SPC

Assembly

Quality control SPC

100 % Final test

Quality control AOQ

Monitoring

Lot release via sampling
Acceptance criterion $c = 0$

SPC: Statistical Process Control
AOQ: Average Outgoing Quality

Stock/customer

Fig. 13
QUALIFICATION AND RELEASE

New wafer processes, packages and device types are qualified according to the internal Vishay Semiconductors specification DQD 3000. DQD 3000 consists of five parts (see figure 18.).

Wafer process release
The wafer process release is the fundamental release qualification for the various technologies used by Vishay Semiconductors. Leading device types are defined for various technologies. Three wafer lots of these types are subjected to an extensive qualification procedure and are used to represent this technology. A positive result will lead to release of the technology.

Package release:
The package release is the fundamental release qualification for the different packages used. Package groups are defined. Critical packages are selected: two assembly lots are subjected to the qualification procedure represented. A positive result will release all similar packages.

Device type release
The device type released is the release of individual designs.

Monitoring
Monitoring serves both as the continuous monitoring of the production and as a source of data for calculation of early failures (early failure rate: EFR).
**Product or process changes** are released via ECN (Engineering Change Note). This includes proving process capability and meeting the quality requirements. Test procedures utilized are IEC 68-2-... and MIL-STD-750 respectively.

**STATISTICAL METHODS FOR PREVENTION**

To manufacture high-quality products, it is not sufficient to inspect the product at the end of the production process. Quality has to be “designed-in” during process and product development. In addition to that, the “designing-in” must also be ensured during production flow. Both will be achieved by means of appropriate measurements and tools.

- Statistical Process Control (SPC)
- R & R- (Repeatability and Reproducibility) tests
- Up-Time Control (UTC)
- Failure Mode and Effect Analysis (FMEA)
- Design Of Experiments (DOE)
- Quality Function Deployment (QFD)

Vishay has been using SPC as a tool in production since 1990/91. By using SPC, deviations from the process control goals are quickly established. This allows control of the processes before the process parameters run out of specified limits. To assure control of the processes, each process step is observed and supervised by trained personnel. Results are documented. Process capabilities are measured and expressed by the process capability index ($C_{pk}$).

Validation of the process capability is required for new processes before they are released for production. Before using new equipment and new gauges in production, machine capability ($C_{mk} = \text{machine capability index}$) or R & R (Repeatability & Reproducibility) is used to validate the equipment’s fitness for use.

Up-Time is recorded by an Up-Time Control (UTC) system. This data determines the intervals for preventive maintenance, which is the basis for the maintenance plan. A process-FMEA is performed for all processes (FMEA = Failure Mode and Effect Analysis). In addition, a design- or product-FMEA is used for critical products or to meet agreed customer requirements.

Design of Experiments (DOE) is a tool for the statistical design of experiments and is used for optimization of processes. Systems (processes, products and procedures) are analyzed and optimized by using designed experiments. A significant advantage compared to conventional methods is the efficient performance of experiments with minimum effort by determining the most important inputs for optimizing the system.

As a part of the continuous improvement process, all Vishay employees are trained in TQM thinking and in using new statistical methods and procedures.

**RELIABILITY**

The requirements concerning quality and reliability of products are always increasing. It is not sufficient to only deliver fault-free parts. In addition, it must be ensured that the delivered goods serve their purpose safely and failure of free, i.e. reliably. From the delivery of the device and up to its use in a final product, there are some occasions where the device or the final product may fail despite testing and outgoing inspection.

In principle, this sequence is valid for all components of a product. For these reasons, the negative consequences of a failure, which become more serious and expensive the later they occur, are obvious. The manufacturer is therefore interested in supplying products with the lowest possible

- AOQ (Average Outgoing Quality) value
- EFR (Early Failure Rate) value
- LFR (Long-term Failure Rate) value

**AVERAGE OUTGOING QUALITY (AOQ)**

All outgoing products are sampled after 2 x 100 % testing. This is known as "Average Outgoing Quality" (AOQ). The results of this inspection are recorded in ppm (parts per million) using the method defined in JEDEC 16.

**EARLY FAILURE RATE (EFR)**

EFRs are an estimate in ppm of the number of early failures related to the number of devices used. Early failures are normally those which occur within the first 300 h to 1000 h. Essentially, this period of time covers the guarantee period of the finished unit.

Low EFR values are therefore very important to the device user. The early life failure rate is heavily influenced by complexity. Consequently, “designing-in” of better quality during the development and design phase, as well as optimized process control during manufacturing, significantly reduces the EFR value. Normally, the early failure rate should not be significantly higher than the random failure rate. EFR is given in ppm (parts per million).

**LONG-TERM FAILURE RATE (LFR)**

LFR shows the failure rate during the operational period of the devices. This period is of particular interest to the manufacturer of the final product. Based on the LFR value, estimations concerning long-term failure rate, reliability and a device’s or module’s operational life may be derived. The usage life time is normally the period of constant failure rate. All failures occurring during this period are random.

Within this period the failure rate is:

$$\lambda = \frac{\text{Sum of failures}}{\Sigma (\text{Quantity} \times \text{Time to failure})} \times \frac{1}{h}$$

The measure of $\lambda$ is FIT (Failures In Time = number of failures in $10^9$ device hours).
Example
A sample of 500 semiconductor devices is tested in an operating life test (dynamic electric operation). The devices operate for a period of 10 000 h.

Failures:
1 failure after 1000 h
1 failure after 2000 h

The failure rate may be calculated from this sample by

\[ \lambda = \frac{2}{1 \times 1000 + 1 \times 2000 + 498 \times 10 000} \times \frac{1}{10 000} \]

\[ \lambda = \frac{2}{4 983 000} \times \frac{1}{h} = 4.01 \times 10^{-7} \frac{1}{h} \]

This is a \( \lambda \)-value of 400 FIT, or this sample has a failure rate of 0.04 %/1000 h on average.

CONFIDENCE LEVEL
The failure rate \( \lambda \) calculated from the sample is an estimate of the unknown failure rate of the lot.
The interval of the failure rate (confidence interval) may be calculated, depending on the confidence level and sample size.
The following is valid:
• The larger the sample size, the narrower the confidence interval.
• The lower the confidence level of the statement, the narrower the confidence interval.
The confidence level applicable to the failure rate of the whole lot when using the estimated value of \( \lambda \) is derived from the \( x^2 \)-distribution. In practice, only the upper limit of the confidence interval (the maximum average failure rate) is used.

Therefore:

\[ \lambda_{\text{max}} = \frac{\chi^2/2(r;\alpha)}{n \times t} \times \frac{1}{10^9 \text{ ln (FIT)}} \]

where:
- \( r \): Number of failures
- \( PA \): Confidence level
- \( n \): Sample size
- \( t \): Time in hours
- \( n \times t \): Device hours

The \( x^2/2 \) for \( \lambda \) are taken from table 1.

For the above example from table 1:
\( x^2/2 (r = 2; \ PA = 60 \%) = 3.08 \)
\( n \times t = 4 983 000 \ h \)

\[ \lambda = \frac{3.08}{4 983 000} = 6.8 \times 10^{-7} \frac{1}{h} \]

This means that the failure rate of the lot does not exceed 0.0618 %/1000 h (618 FIT) with a probability of 60 %.

If a confidence level of 90 % is chosen from table 1:
\( x^2/2 (r = 2; \ PA = 90 \%) = 5.3 \)

\[ \lambda_{\text{max}} = \frac{5.3}{4 983 000} = 1.06 \times 10^{-6} \frac{1}{h} \]

This means that the failure rate of the lot does not exceed 0.106 %/1000 h (1060 FIT) with a probability of 90 %.

TABLE 1

<table>
<thead>
<tr>
<th>NUMBER OF FAILURES</th>
<th>50 %</th>
<th>60 %</th>
<th>90 %</th>
<th>95 %</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.60</td>
<td>0.93</td>
<td>2.31</td>
<td>2.96</td>
</tr>
<tr>
<td>1</td>
<td>1.68</td>
<td>2.00</td>
<td>3.89</td>
<td>4.67</td>
</tr>
<tr>
<td>2</td>
<td>2.67</td>
<td>3.08</td>
<td>5.30</td>
<td>6.21</td>
</tr>
<tr>
<td>3</td>
<td>3.67</td>
<td>4.17</td>
<td>6.70</td>
<td>7.69</td>
</tr>
<tr>
<td>4</td>
<td>4.67</td>
<td>5.24</td>
<td>8.00</td>
<td>9.90</td>
</tr>
<tr>
<td>5</td>
<td>5.67</td>
<td>6.25</td>
<td>9.25</td>
<td>10.42</td>
</tr>
<tr>
<td>6</td>
<td>6.67</td>
<td>7.27</td>
<td>10.55</td>
<td>11.76</td>
</tr>
<tr>
<td>7</td>
<td>7.67</td>
<td>8.33</td>
<td>11.75</td>
<td>13.16</td>
</tr>
<tr>
<td>8</td>
<td>8.67</td>
<td>9.35</td>
<td>13.00</td>
<td>14.30</td>
</tr>
<tr>
<td>9</td>
<td>9.67</td>
<td>10.42</td>
<td>14.20</td>
<td>15.63</td>
</tr>
<tr>
<td>10</td>
<td>10.67</td>
<td>11.42</td>
<td>15.40</td>
<td>16.95</td>
</tr>
</tbody>
</table>
OPERATING LIFE TESTS
Number of devices tested: n = 50
Number of failures: (positive qualification): c = 0
Test time: t = 2000 h
Confidence level: PA = 60 %
\[ \frac{x^2}{2} (0; 60 \%) = 0.93 \]

\[ \lambda_{\text{max}} = \frac{0.93}{50 \times 2000} = 9.3 \times 10^{-6} \frac{1}{h} \]

This means, that the failure rate of the lot does not exceed 0.9 %/1000 h (9300 FIT) with a probability of 60 %.
This example demonstrates that it is only possible to verify LFR values of 9300 FIT with a confidence level of 60 % in a normal qualification test (50 devices, 2000 h).
To obtain LFR values which meet today’s requirements (< 50 FIT), the following conditions have to be fulfilled:
• Very long test periods
• Large quantities of devices
• Accelerated testing (e.g. higher temperature)

MEAN TIME TO FAILURE (MTTF)
For systems which cannot be repaired and whose devices must be changed, e.g. semiconductors, the following is valid:

\[ \text{MTTF} = \frac{1}{\lambda} \]

MTTF is the average fault-free operating period per a monitored (time) unit.

ACCELERATING STRESS TESTS
Innovation cycles in the field of semiconductors are becoming shorter and shorter. This means that products must be brought to the market quicker. At the same time, expectations concerning the quality and reliability of the products have become higher.
Manufacturers of semiconductors must therefore assure long operating periods with high reliability but in a short time. Sample stress testing is the most commonly used way of assuring this.
The rule of Arrhenius describes this temperature dependent change of the failure rate.

\[ \lambda (T_2) = \lambda (T_1) \times e^{\frac{E_A}{k} \left( \frac{1}{T_1} - \frac{1}{T_2} \right)} \]

Boltzmann’s constant
\[ k = 8.63 \times 10^{-5} \text{ eV/K} \]
Activation energy
\[ E_A \text{ in eV} \]
Junction temperature real operation
\[ T_1 \text{ in Kelvin} \]
Junction temperature stress test
\[ T_2 \text{ in Kelvin} \]
Failure rate real operation
\[ \lambda (T_1) \]
Failure rate stress test
\[ \lambda (T_2) \]
The acceleration factor is described by the exponential function as being:

\[ \text{AF} = \frac{\lambda (T_2)}{\lambda (T_1)} = e^{\frac{E_A}{k} \left( \frac{1}{T_1} - \frac{1}{T_2} \right)} \]

Example
The following conditions apply to an operating life stress test:
Environmental temperature during stress test
\[ T_A = 70 \degree C \]
Power dissipation of the device
\[ P_V = 100 \text{ mW} \]
Thermal resistance junction/environment
\[ R_{\text{thJA}} = 300 \text{ K/W} \]
The system temperature/junction temperature results from:
\[ T_J = T_A + R_{\text{thJA}} \times P_V \]
\[ T_J = 70 \degree C + 300 \text{ K/W} \times 100 \text{ mW} \]
\[ T_J = 100 \degree C \]
Operation in the field at an ambient temperature of 50 \degree C and at an average power dissipation of 80 mW is utilized.
This results in a junction temperature in operation of
\[ T_J = 74 \degree C \]. The activation energy used for opto components is
\[ E_A = 0.8 \text{ eV} \].
The resulting acceleration factor is:

\[ \text{AF} \approx 6.5 \]
This signifies that, in this example, the failure rate is lower by a factor of 6.5 compared to the stress test.
Other accelerating stress tests may be:
• Humidity (except displays type TDS.)
  \[ T_A = 85 \degree C \]
  \[ \text{RH} = 85 \% \]
• Temperature cycling
  Temperature interval as specified
The tests are carried out according to the requirements of appropriate IEC-standards (see also chapter “Qualification and Release”).
ACTIVATION ENERGY

There are some conditions which need to be fulfilled in order to use Arrhenius' method:

- The validity of Arrhenius' rule has to be verified
- “Failure-specific” activation energies must be determined

These conditions may be verified by a series of tests. Today, this procedure is generally accepted and used as a basis for estimating operating life. The values of activation energies can be determined by experiments for different failure mechanisms.

Values often used for different device groups are:

- Opto components: 0.8 eV
- Bipolar ICs: 0.7 eV
- MOS ICs: 0.6 eV
- Transistors: 0.7 eV
- Diodes: 0.7 eV
- Sinterglass Diodes: 0.7 eV

By using this method, it is possible to provide longterm predictions for the actual operation of semiconductors even with relatively short test periods.

Fig. 17 - Acceleration Factor for Different Activation Energies
Normalized to $T_J = 55 \, ^\circ C$