

Phototriac dV/dt Application Note

Introduction

Phototriacs are used to provide optical isolation between the input (driving source) and output circuits (load). The zero cross (ZC) and non zero cross (NZC) phototriacs are used for interface applications between low current DC and high power AC loads. In many applications, use of ZC TRIAC will eliminate/minimize current surges that result in electromagnetic interference (EMI) and radio frequency interference (RFI).

However, when using TRIACs to drive inductive loads, certain parameter will need to be paid special attention to. This is due to the fact that when driving inductive loads, the voltage and current will not be in phase with one another. Hence, static and commutating dV/dt will need to be considered when using phototriacs.

Vishay provides a broad family of phototriacs. These phototriacs, such as VO425X and VO415X, are capable of satisfying different test levels of the EN61000-4-4 standard. Vishay's IL420, IL410, IL421X, and IL411X series are capable of meeting the highest test level (4kV) for electrical fast transient immunity per EN61000-4-4.

TRIAC dV/dt Types

One set of parameters which deserves special attention when discussing the design of thyristors, and TRIACs in particular, is output dV/dt. This parameter falls into two different categories: static output dV/dt and commutating dV/dt (also see Phototriac Application Note). Each of these output load dV/dt parameters is governed by a different cause and effect.

Static dV/dt

Static dV/dt is the behavior by which a thyristor can be triggered as a result of a high slew rate transient (noise) on the output load, even without any triggering signal ($I_F = 0$) on the input. The mechanism by which this type of false triggering takes place is a coupling of the high-frequency transient output noise back to the gate by means of parasitic coupling capacitances, as illustrated in Figure 1. The measurement technique for static dV/dt is illustrated in Figure 2.

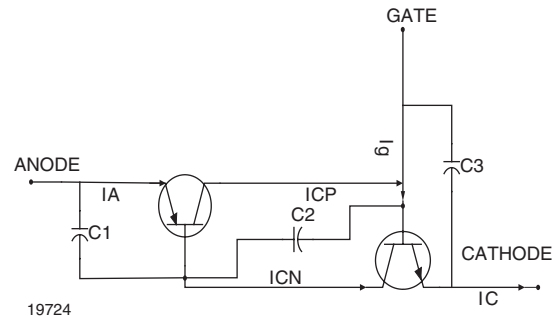


Figure 1. SCR Parasitic Capacitance

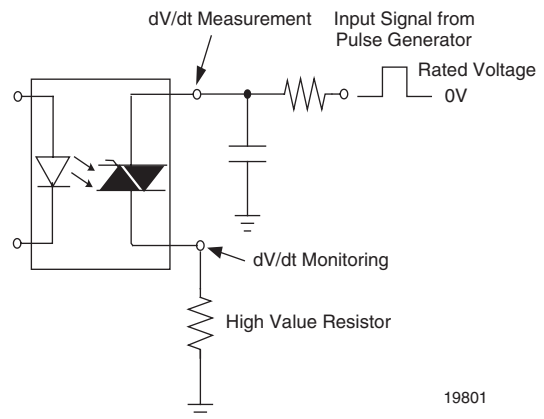


Figure 2-a. dV/dt Measurement Technique

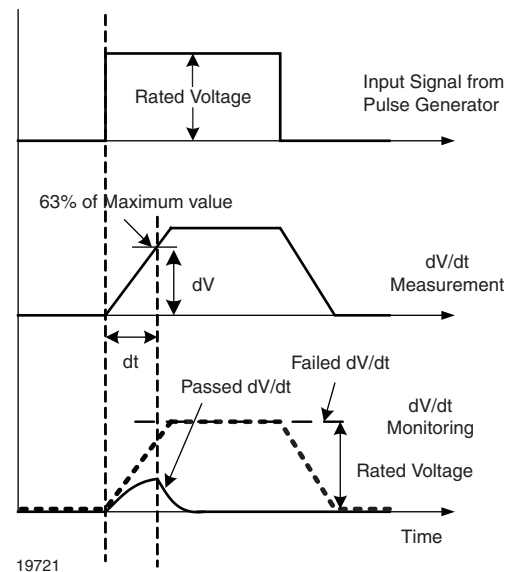


Figure 2-b. dV/dt Measurement

Manufacturers typically provide static dV/dt numbers in datasheets and specify them in $V/\mu s$. They can range from tens of volts/ μs up to 10 $kV/\mu s$, as in the case of the IL410 or IL420. The IL410 (zero-crossing) and IL420 (non-zero crossing) phototriacs offer the highest dV/dt performance in the industry at 10 $kV/\mu s$.

Commutating dV/dt

Commutating dV/dt is not a design parameter that comes into play in inadvertent turn-on. Instead it prevents the TRIAC from turning off. It is important to note that TRIAC commutating dV/dt issue comes into play during turn off (TRIAC turns off after I_F makes its transaction from high value to zero and at the zero current crossing of the AC current through it.)

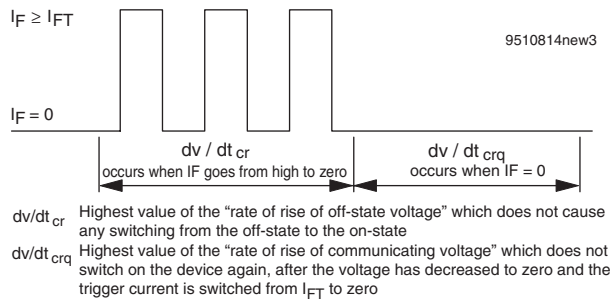


Figure 3. Static and Commutating dV/dt

Figure 3 shows one way to look at the difference between commutating and static dV/dt . The right-hand portion of the waveform in Figure 3 labeled dV/dt_{crq} refers to the static dV/dt or the maximum pulse rise time required to turn a TRIAC on from an off-state. The left-hand part of Figure 3 illustrates the condition under which commutating dV/dt (dV/dt_{cr}) occurs. This describes how long the TRIAC has to be off to ensure that the device will stay off, since it is not desired to have the voltage across the TRIAC to rise while the current through TRIAC is crossing zero.

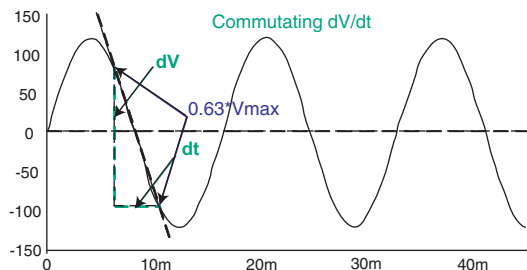


Figure 4. dV/dt Measurement

Figure 4 describes a practical approach to measuring the commutating dV/dt parameter. In other words, what is the maximum sinusoidal frequency that a TRIAC can see before it no longer can be turned off once it is triggered. In practice this is probably the easiest way to measure commutating dV/dt . The only thing required is an AC source of sufficient voltage and frequency range.

In the case of inductive loads, dV/dt is of primary importance, because the effective commutating dV/dt is very tightly related to the power factor of the load. This is illustrated in Figure 5-a, and understanding it simply requires the reader to go back to the "ELI the ICE man" rule of basic electronics (ELI is used to represent the fact that the inductor voltage leads the inductor current. ICE is used to represent the fact that the capacitor current leads the capacitor voltage). If the current lags the voltage, such as is the case in an inductive load, by the time the current crosses zero and the TRIAC turns off, there is already a significant voltage across the device, and it is immediately time to turn on again. Therefore the device never has enough time to clear out the charge in the gate region and simply stays on cycle after cycle. This phenome-

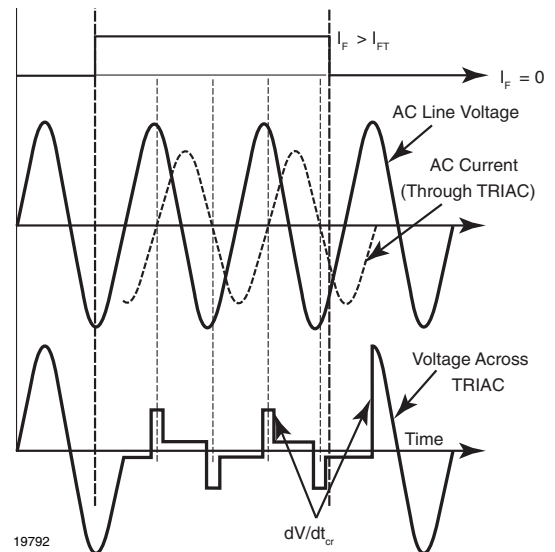


Figure 5-a. Inductive Load and Commutating dV/dt

non manifests itself in the load device turning on and failing to turn off for one or more cycles after the first zero crossing when the gate signal is removed.

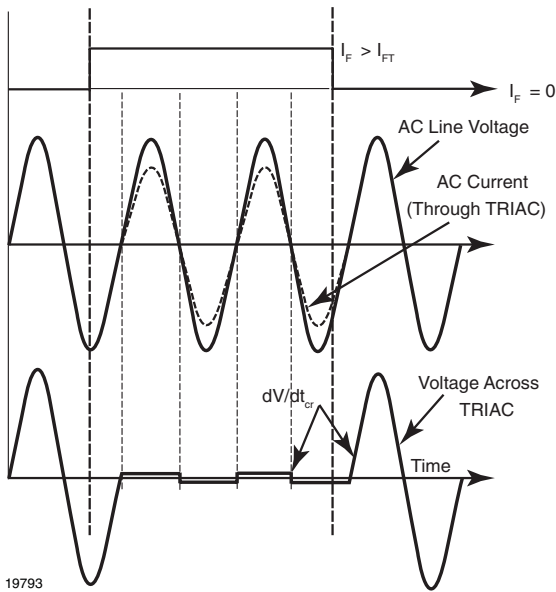


Figure 5-b. Resistive Load and Commutating dV/dt

Resistive Versus Inductive Load Applications

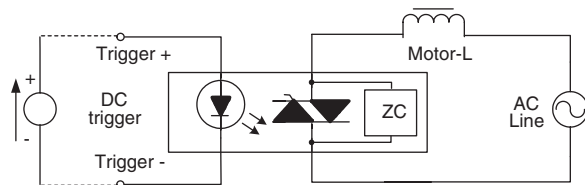
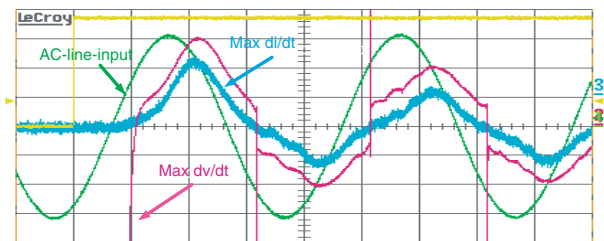
In cases where simple resistive loads are controlled, the dV/dt of the load is not usually a major concern; however, the main restriction is that the TRIAC must be properly chosen to sustain the proper inrush current and perhaps be protected by a fuse. Many loads that utilize TRIAC control are inductive loads where high rates of dV/dt and di/dt require design control schemes that can contend with these high slew rate conditions. Figures 6-a and 6-b (as well as Figures 8 and 9) show the maximum dV/dt and di/dt location on the voltage curve across TRIAC and AC current through TRIAC.

A perfect example of inductive load is a TRIAC application where the load is an electric motor. Electric motors, like any inductive load, have lagging displacement power factors associated with them (the inductive load's voltage leads its current). This presents a unique problem with TRIAC circuits, in that there is a limitation to how fast the load voltage can change and still allow sufficient time for the TRIAC to turn off. This is not something that is encountered with simple SCRs, where the SCR has an entire half cycle to discharge the gate region; however, in the case of TRIACs the amount of time allowed for gate-region discharge is only a very small period around the zero-current crossing point.

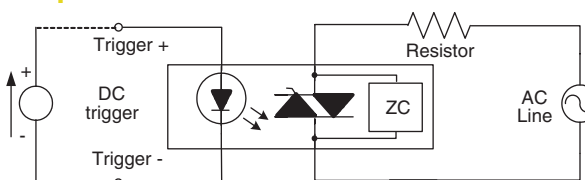
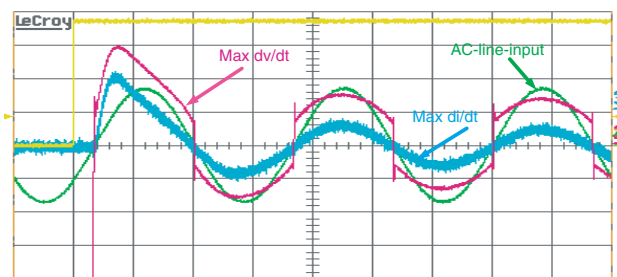
In the case of an inductive load, the turn-off region of a TRIAC is pushed out beyond the zero-voltage crossing point of the TRIAC. Consequently, when the

TRIAC finally turns off, the voltage is not at or near zero but something much higher. This leads to the dV/dt across the TRIAC being much higher than would be in the case of resistive loads where the current and voltage were in phase. Figures 5-a and 5-b show the TRIAC voltage and current when driving inductive and resistive load (at commutation).

Both the resistive and inductive load applications are shown in Figures 6-a and 6-b, which illustrates the detrimental affect of power factor on commutating dV/dt. Notice the difference in the magnitude of the dV/dt spikes between the inductive and resistive load applications. In the case of the inductive load, the voltage is already significantly higher than zero before the current even gets to the zero point. This results in even less than normal time being available for minority charge carriers to be cleared from the gate region.



Inductive Load without snubber
Figure 6-a. Inductive Load Without Snubber



Resistive Load
Figure 6-b. Resistive Load.

Solutions to dV/dt Triggering

Whether the effects are due to static dV/dt triggering or commutating dV/dt, as described above, and though the results are different, the possible solutions are similar. The options are to either reduce the effective dV/dt experienced across the TRIAC or to utilize a TRIAC that is capable of withstanding high dV/dt transitions. As we will see, the choice between these approaches depends largely on economics and available board real estate.

The first approach is to reduce the dV/dt seen by the TRIAC. This involves implementing an RC snubber circuit across the load, such as the circuit illustrated in Figure 7.

The fundamental governing equation involved is as follows:

$$Ri + L \frac{di}{dt} + \frac{1}{C} \int idt + V_0 = 0$$

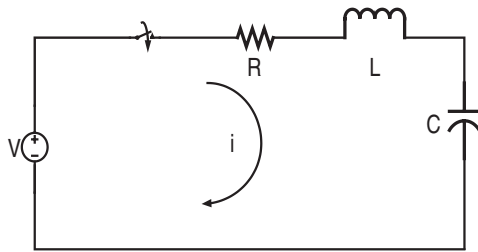


Figure 7. Simplifies TRIAC Circuit With Snubber

This equation is derived from the governing differential equation describing an RLC series circuit, as illustrated above.

From this basic equation one can derive the equations required to calculate the desired snubber values.

β is the damping factor for the RLC resonant waveform, and 0.7 is a good rule of thumb number to use

$$C = \frac{1}{\omega_0^2 L}$$

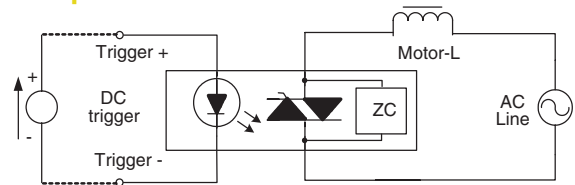
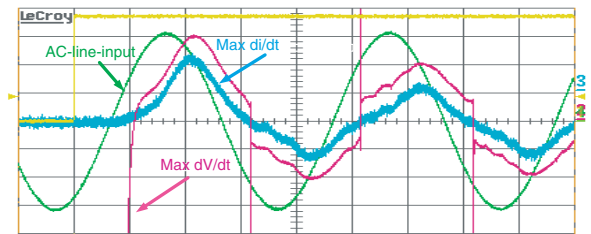
$$R = \frac{\beta}{\omega_0 C}$$

$$\frac{dV}{dt} = \frac{VR}{L}$$

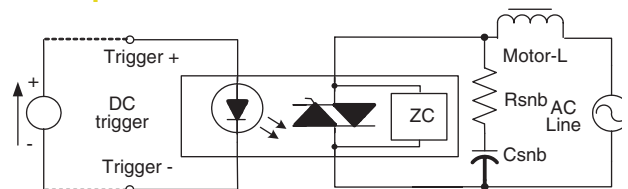
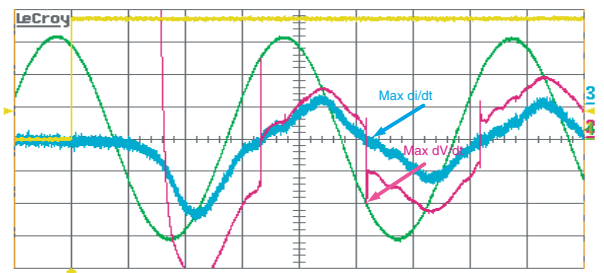
for this value; however, lower values can be used if more damping is required for the resonant peak. And dV/dt refers to the maximum permissible load slew rate for a particular device.

The process of designing the snubber may be straightforward on the conceptual level, but in practice it turns out to be a somewhat empirical and iterative process, since design objectives always need to be reconciled with the capabilities of real off-the-shelf components.

The decrease in dV/dt through the use of a snubbing technique is illustrated in the example in Figures 8 and 9. Figure 8 illustrates an inductive load lacking a snubber and possessing extreme dV/dt spikes on the voltage curve across the TRIAC, which are labeled “max dV/dt.” Figure 9 demonstrates the dampening effect of introducing a snubber circuit at the output of the TRIAC device. The difference in the amplitude of the maximum dV/dt spikes is accounted for by the snubbing effect of the RC network.



Inductive Load without snubber
Figure 8. Inductive Load Without Snubber



Inductive Load with snubber
Figure 9. Inductive Load With Snubber



Vishay Semiconductors

Instead of resorting to a snubber and a low dV/dt TRIAC, another approach that offers the designer a compact, high-performance solution is a TRIAC driver with extremely large dV/dt immunity, such as a Vishay IL410, or IL420. This will allow the designer to create a TRIAC application while avoiding entirely the need for lossy, large, and possibly expensive snubber circuits. Vishay's high dV/dt phototriacs come in both non-zero and zero crossing configurations and have dV/dt ratings as high as $10000\text{ V}/\mu\text{s}$. These high dV/dt ratings eliminate the need for snubber circuits in most cases and greatly diminish the size of the required components that are needed except in extreme cases involving poor power factor control. Phototriac drivers enable a compact and elegant solution with improved performance, smaller PCB space, and often lower price.