Optocoupler VOT8121, Phototriac Output, Non-Zero Crossing

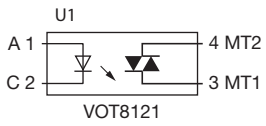
DESCRIPTION

This device VOT8121 consists of a GaAs IRLED optically coupled to a photosensitive TRIAC packaged in a DIP-4 package.

The PSpice models have been written from device characterization data and were tested with simulation program OrCAD16.6.

The symbol and model files as well as the netlist are in the symbol library file VOT8121.olb, model library file VOT8121.lib, and netlist file VOT8121.txt respectively for this model.

This document is intended as a guideline of simulating with provided model and does not constitute as commercial product, neither a substitute to datasheet.

PART	MODEL DESCRIPTION	SYMBOL FILE	MODEL FILE
VOT8121	Phototriac	 VOT8121.olb	VOT8121.lib

RECOMMENDED USE OF THE MODEL

- This model is designed only for use at 25 °C and should be used as is
- This model has been created and tested with OrCAD version 16.6
- The olb file (symbol) is not down-compatible. Users of the earlier versions need to create the symbols on their platform and associate with relative PSpice model data

NETLIST OF MODEL

Following list shows the netlist of the model:

```
* Library of Phototriac Optocoupler VOT8121
* Copyright VISHAY, Inc. 2018 All Rights Reserved.

.SUBCKT VOT8121 A C MT2 MT1
X1        MT1 GATE MT2 VOT8121_tr
D1        10 C Demit
V3        11 10 0Vdc ; emitter current probe
R3        A 11  1u TC=0,0
*R4         0 NC 1MEG
*C1         0 NC 1u
G1        0 GATE VALUE { I(v3) * 0.51 }
.MODEL Demit d
+IS=5.60248e-15 RS=1.43261 N=1.58216 EG=1.3
+XTI=3.75582 BV=6 IBV=5e-6 CJO=1e-11
+VJ=0.7 M=0.5 FC=0.5 TT=1e-09
```

```
+KF=0 AF=1
.ENDS
**************
.SUBCKT VOT8121_tr  3 2 1
*     TERMINALS: MT1 G MT2
QN1  5 4 3  NOUT OFF
QN2 11 6 7  NOUT OFF
QP1 6 11 3  POUT OFF
QP2  4 5 7  POUT OFF
DF  4  5  DZ
DR  6 11  DZ
RF  4 6  60.0G
RT2 1 7  0.45
RH  7 6  18.75k
RGP 8 3  102
RG  2 8  998
RS  8 4  3.65k
DN  9 2  DIN
RN  9 3  855k
GNN  6 7 9 3 24.3u
GNP  4 5 9 3 26.5u
DP 2 10  DIP
RP 10 3  110k
GP  7 6 10 3 20.5u
.MODEL DIP D ( IS=1.07f N=1.50 )
.MODEL DIN D ( IS=1.07f )
.MODEL DZ D ( IS=1.07f N=1.5 IBV=10.0n BV=800 )
.MODEL POUT PNP ( IS=1.07f BF=5 BR=.1 CJE=35f TF=1.8u )
.MODEL NOUT NPN  ( IS=1.07f BF=20 BR=.1 CJE=35f CJC=67.0f TF=1.080u )
.ENDS

**************
**=====================================================================*
* Note:                                                               *
* Although models can be a useful tool in evaluating device           *
* performance, they cannot model exact device performance             *
* under all conditions, nor are they intended to replace              *
* breadboarding for final verification!                               *
*                                                                     *
* Models provided by VISHAY Semiconductors GmbH are not               *
* as fully representing all of the specifications and operating       *
* characteristics of the semiconductor product to which the           *
* model relates.                                                      *
* The models describe the characteristics of typical devices.         *
* In all cases, the current data sheet information for a given        *
* device is the final design guideline and the only actual            *
* performance specification.                                          *
* VISHAY Semiconductors does not assume any liability arising         *
* from the model use. VISHAY Semiconductors reserves the right to     *
* change models without prior notice.                                 *
**=====================================================================*
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SIMULATED PARAMETERS (T_{amb} = 25 °C, unless otherwise specified)				
PARAMETER	**TEST CONDITION**	**SYMBOL**	**SIMULATION DATA**	**UNIT**
INPUT				
Forward voltage	I_F = 20 mA	V_F	1.21	V
Trigger input current	V_T = 3 V	I_{FT}	10	mA
OUTPUT				
Repetitive peak off-state voltage		V_{DRM}	800	V

EXAMPLE SIMULATION PLOTS USING OrCAD

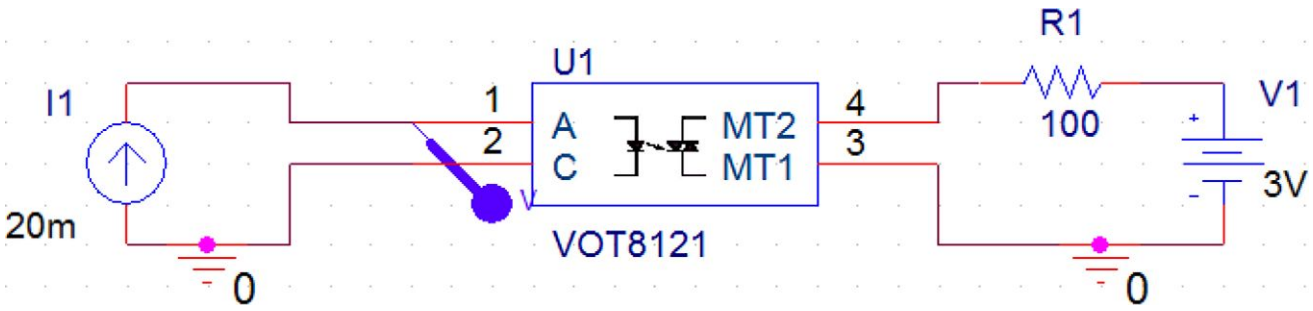

Fig. 1 - Simulation Setup for V_F vs. I_F Curve

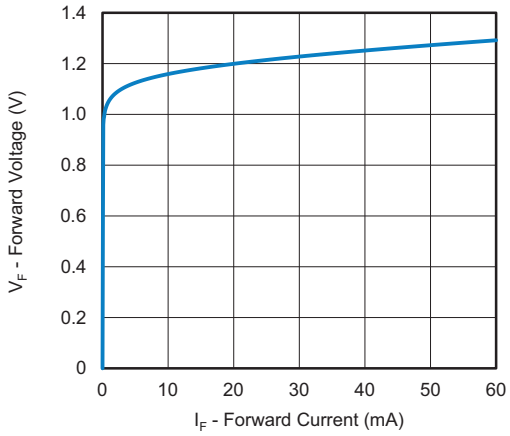

Fig. 2 - Forward Voltage vs. Forward Current

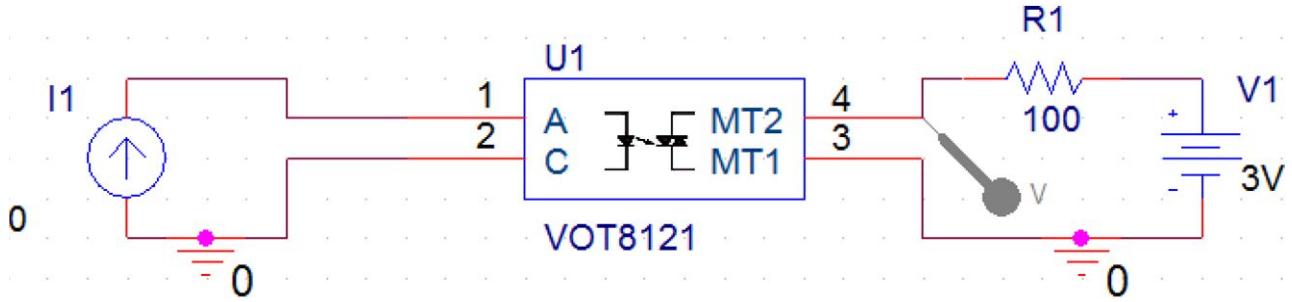

Fig. 3 - Simulated Setup for I_{FT} and V_{DRM} Parameters

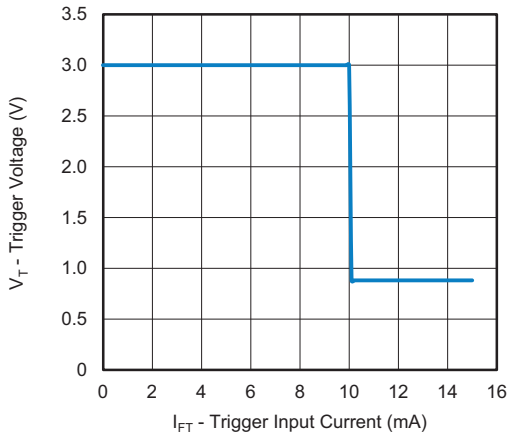

Fig. 4 - Trigger Voltage (V_T) vs. Trigger Input Current (I_{FT})

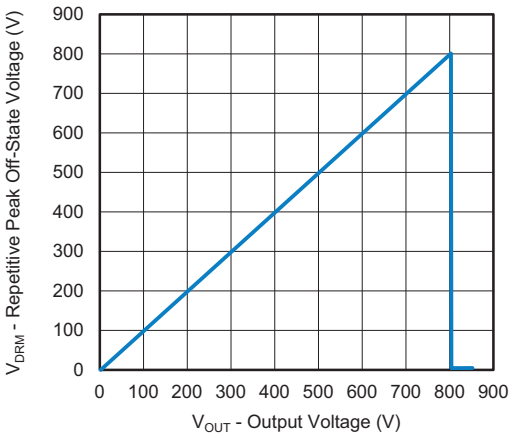

Fig. 5 - Repetitive Peak Off-State Voltage (V_{DRM})