

ESD Protection: I/O Port Designers Look to Protect Against ESD Threats

*By Jon Schleisner
Senior Applications Engineer*

Reliability has become an essential component of any communication and data management system. In some regions of the global marketplace these reliability standards are government imposed. This is particularly true in Europe where the IEC (International Electrotechnical Commission) is very influential. North America has Canadian Standards Association and Underwriters Laboratories. Most of the time, system reliability is demanded by the consumer. Communication and data management systems are the backbone of modern business and down time costs money.

Whether government imposed or customer demanded, reliability (and perceived quality) is here to stay. Enter the ESD protection of data ports. P.C.'s, printers and LAN's all have one thing in common. Each one must interface with other existing hardware in order to perform their required tasks. The designers of P.C.'s, printers, LAN hubs, data entry terminals and "black box interfaces" all face a common problem; ESD surge events at the interface from the outside world. These surges must be dealt with in an efficient and cost effective manner.

Vishay offers several TVS Array solutions. The traditional method of protecting data ports against ESD is to use RC filters or individual Zener diode clamps to limit the voltage excursions at the data port to safe levels. These are levels that will not damage the transceiver chips or cause latch up and require system restart to recover the data port. Filters and zener clamps are effective solutions, but often prove expensive from both a cost and board real estate point of view. By contrast, the TVS Array solution is an extremely cost effective solution and the footprint of the device (in SOIC form) is extremely compact. This package style is small enough to fit comfortably on the rear of a printed circuit board between the input connector shell and the associated transceiver circuit.

Measuring the performance of ESD protection devices is an arduous task. Due to the extremely fast rise time (on the order of 10kv/ns) recording these events requires

sophisticated (and expensive) test equipment. In this case, the test pulse was applied with the KeyTek minizap model MZ15/EC with TPC-2 tip. The events were recorded with a Tektronics SCD1000 transient waveform recorder.

This scope has the capability of performing ultra high speed differential measurements and storing the information. The difficult part of the measurement is developing a test fixture that will support the SMD component and allow a reasonably clean, high speed measurement.

The test fixture breaks with tradition as it mounts directly on the front panel inputs of the scope. The internal 50 ohm impedance of the scope is used in conjunction with 1K Ω low inductance carbon resistors to form wide band attenuators between the scope and the test fixture interface. The attenuation factor is 21:1.

Figure 1 shows the test fixture. The attenuators are mounted directly on the double sided printed circuit board which supports the DUT. 1K Ω resistors (hand matched to 0.25% of each other) are mounted directly on the chassis mount male BNC connectors. The other end of the resistors are measurement points. Schematic 1 shows the measurement circuit. The purpose of the differential measurement technique is to provide noise cancellation across the ground plane.

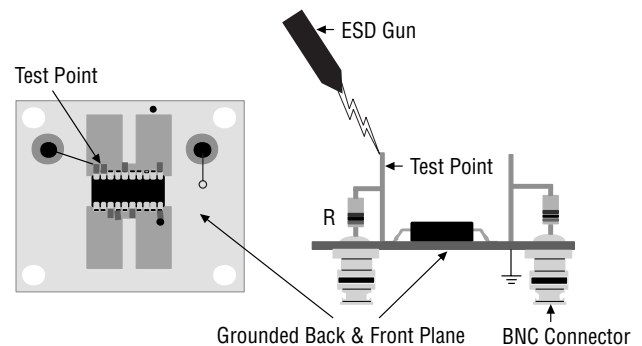
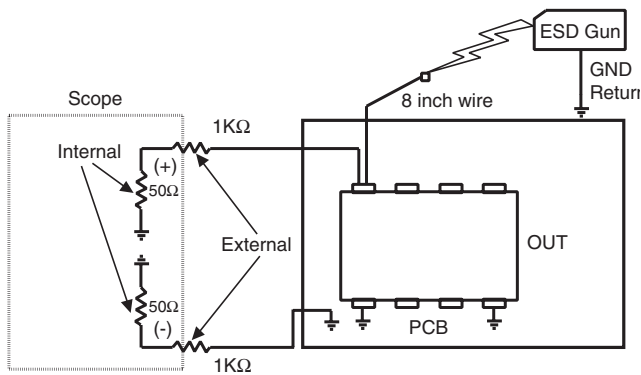


Fig. 1

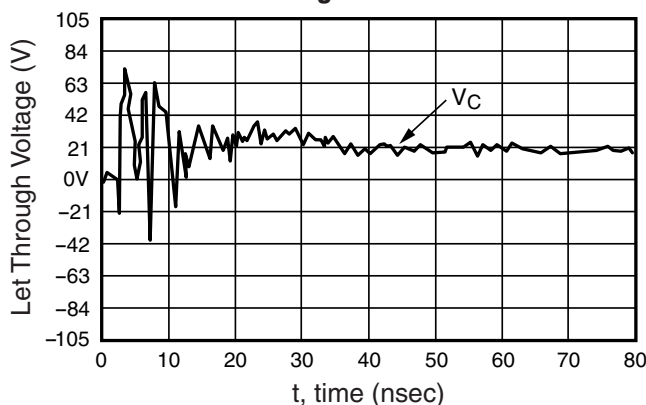


Schematic 1

The ESD pulse is supplied via the KeyTek minizap gun with direct application via an 8 inch jumper wire. The wire is necessary to reduce the residual noise level around the scope and prevent false triggering. Figure 2 shows the response of a bidirectional array with an 8kV spike applied to an input pin. Figure 3 shows the response to an 8 kV spike in the negative direction.

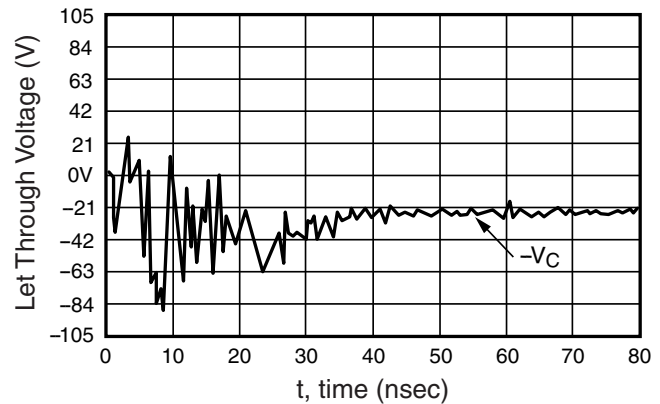
The initial leading edge of the pulse shows the “let thru” voltage due to the inductance in the circuit board and internal wire bonds in the package. This settles out after roughly 20 ns and the array can be seen to clamp at V_C . The measured “let thru” voltage is less than 100 volts in either direction. In a perfect world, the voltage peak would not exceed the clamping level, but circuit board and packaging limitations cause the initial “let thru” voltages. The energy level during the “let thru” period of the waveform is very low and delivers minimal stress to the protected port. It is possible to design a protector with almost zero

Fig. 2 – Typical Response to 8KV Positive Going ESD Pulse

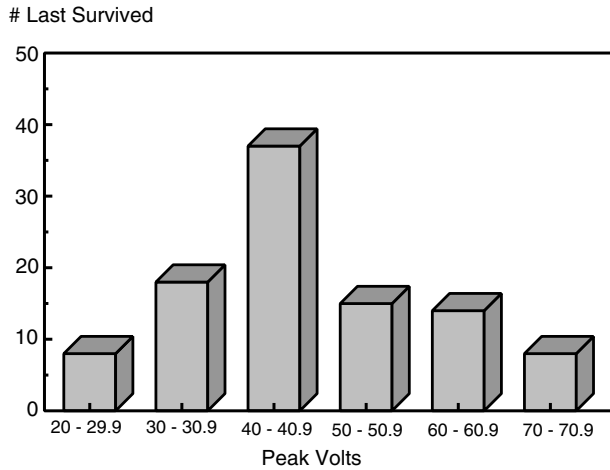


“let thru”. However this would require “kelvin” (or 4 point) connections to each signal line node. This would mean that an eight line package could protect only 2 lines. This would result in a very expensive solution that few engineers could afford to design in.

Fig. 3 – Typical Response to 8KV Negative Going ESD Pulse

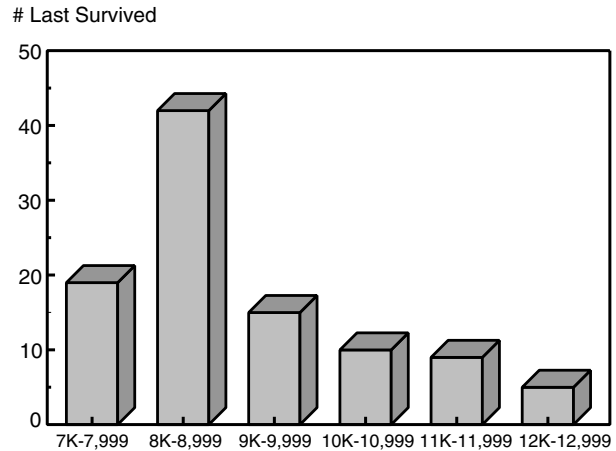


While these pictures are interesting, they deliver only implied proof that TVS Array devices provide protection against ESD pulses. For a more conclusive demonstration it is necessary to use the array devices in a circuit protecting an ESD sensitive component. At Vishay, we have access to a substantial store of small geometry power MOSFETs in TO-92 cases. These MOS devices proved to be an ideal candidate for an ESD “stress to failure” test. All ESD test pulses were delivered by the KeyTek minizap gun. Graph 1 provides data on a 100 piece sample. The voltages indicated are the ESD voltages the devices last survived. This first group of 100 pieces were tested without any protection devices in place. They were soldered onto printed circuit board ground planes with the source and drain tied to ground and the gate floating. It can be seen in Graph 1, that the devices all failed below 100V. This made these particular MOSFETs an ideal candidate to test the functional effectiveness of the TVS Array.



Graph 1

The second set of 100 pieces were soldered onto test boards with the source and drain connected to the ground plane and the gate attached to one input line on the TVS array. The same procedure was used stepping 20 volts at a time. At the 100V level, it was observed that all 100 devices had survived. The incremental level was then increased in 500V steps. The results appear on Graph 2, which show MOSFETs gate rupture at a minimum of 7.5 kV and a maximum of 12.0 kV. This is outstanding ESD immunity.



Graph 2

Certainly the TVS Array product provides greatly enhanced ESD performances verses the unprotected FETs. One of the critical parameters influencing the effectiveness of TVS Arrays, or other protection technologies, is placement. Inductance on the ground-return circuit will dramatically decrease the TVS performance against ESD. The extremely fast rise times observed during ESD events make proper suppressor placement a necessity not an elegant option.