Protection Diodes | Application Note

Selecting Automotive Power Line Polarity Protection Diodes

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A major challenge in automotive design is protecting electronics - such as control units, sensors, and entertainment systems - against damaging reverse voltages, voltage transients, electrostatic discharge (ESD), and noise that are present on the power line. Rectifiers are ideal solutions for automotive electronic power line protection and have several important parameters for these applications, including forward current, repetitive reverse voltage, forward surge current, and fusing rate.

PARAMETERS IN AUTOMOTIVE ELECTRONIC EQUIPMENT TEST CONDITIONS AND APPLICATIONS

Basic circuits for polarity protection are shown in Fig 1. Circuit (A) offers polarity protection only, while circuit (B) features polarity protection with load dump suppression.

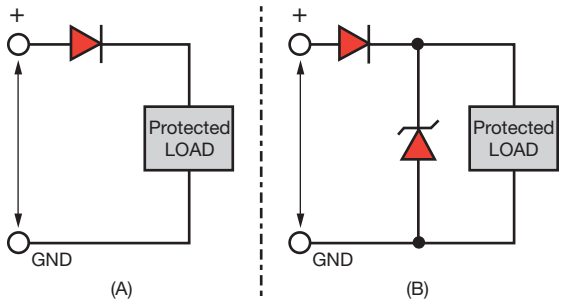

Fig. 1 - Basic Polarity Protection Circuits

Following are definitions for major parameters to consider when selecting a power line polarity protection diode for your automotive application.

Maximum Repetitive Reverse Voltage (V_{RRM})

The maximum repetitive reverse voltage is the maximum voltage that the diode can withstand in reverse bias mode. In reverse bias mode, leakage current through the diode can generate heat in the diode junction and lead to thermal runaway. Tests that simulate this condition include the U.S.'s ISO-7637-2 pulse 1 and 3a, and Japan's JASO D001-94, standard type B and E. Each peak voltage for these tests is specific in the folowing tables and figures.

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TABLE 1: ISO-7637-2, PULSE 1									
SYSTEM (V)	U_S (V)	R_i (Ω)	t_d (ms)	t_r (µs)	t_1 (s)	t_2 (ms)	t_3 (µs)	BURST CYCLE/ PULSE REPITITION TIME (s)	TEST PULSES
12	- 75 to - 150	10	2	1	> 0.5	200	< 100	Min. 0.5	500
24	- 300 to - 600	50	1	3					

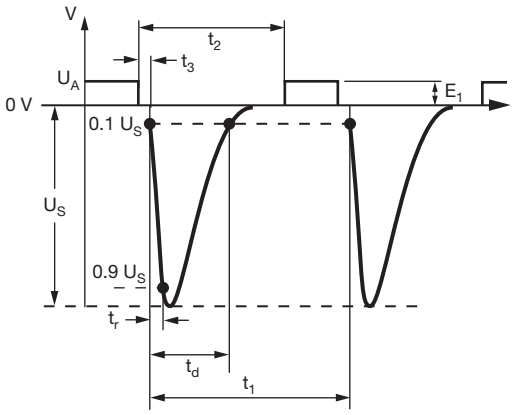

Fig. 2 - ISO-7637-2, Pulse 1

TABLE 2: ISO-7637-2, PULSE 3a									
SYSTEM (V)	U_S (V)	R_i (Ω)	t_d (ns)	t_r (ns)	t_1 (µs)	t_4 (ms)	t_5 (ms)	BURST CYCLE/ PULSE REPITITION TIME (s)	TEST TIME (h)
12	- 112 to - 220	50	150	5	100	10	90	min. 90 to max. 100	1
24	- 150 to - 300								

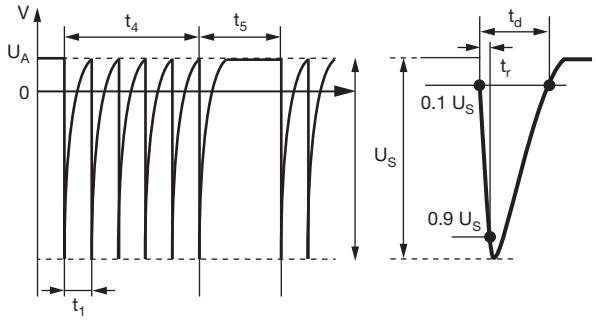

Fig. 3 - ISO-7637-2, Pulse 3a

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TABLE 3: JASO D001-94							
CLASSIFICATION	TYPE OF TEST		V_p (V)	t_d (µs)	f (Hz)	R_i (Ω)	NUMBER OF PULSES
12 V system	Type	B-1	- 80	60 000	1/30	8	100
		B-2	- 250	2000		80	100
24 V system		E	- 320	26 000		210	100

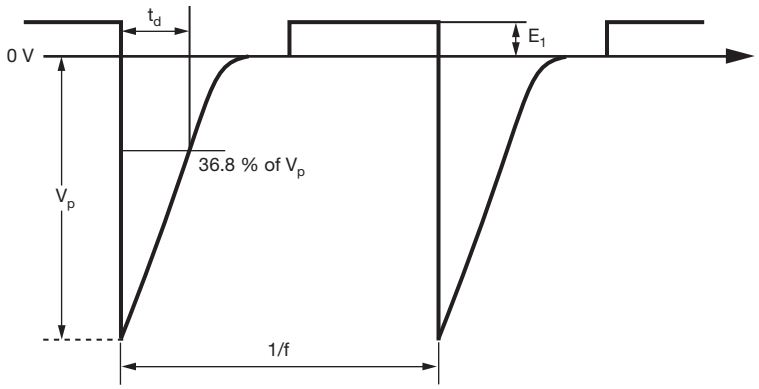

Fig. 4 - JASO D001-94 Type B and E

According to the above test conditions, the V_{RRM} of a diode for power line protection should be 300 V to 400 V for a 12 V power train and 600 V for a 24 V power train.

Forward Current ($I_{F(AV)}$)

The specification for forward current in datasheets usually means the maximum average forward current the diode can handle in the forward bias state, given the thermal limitations of the package. This parameter is related to the current usage of the circuit in operation.

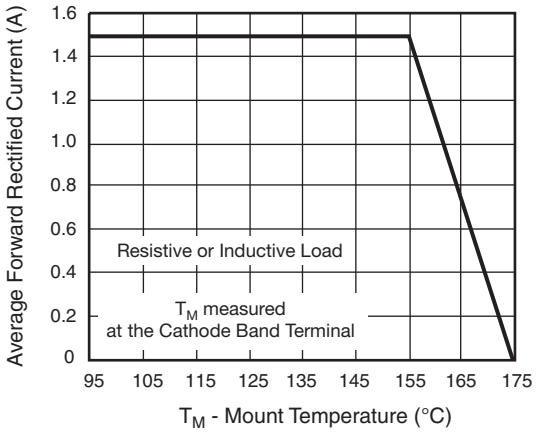

Fig. 5 - The Maximum Forward Current Derating Curve of an AS1P on a 5 mm x 5 mm Cu Pad with a FR-4 PCB

The forward current capability varies by the temperature of the diode's junction, as show in Fig 5. Other related parameters include thermal resistance with the symbols $R_{\theta JC}$, $R_{\theta JA}$, $R_{\theta JL}$, and $R_{\theta JM}$.

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Forward Surge Current (I_{FSM})

The specified forward surge current in a datasheet is the maximum peak current the diode can handle in the forward bias state within specified time and pulse conditions. This rating is limited by the diode's thermal capacity.

The forward surge current specification is related to two major operations and is simulated in the ISO-16750-2 and JASO D001-94 automotive standards. The first operation is protecting circuitry against the high currents that occur during the load dump condition. The second operation is simulated by ISO-7637-2 test pulse 2a and 3b, consisting of 50 ms and 100 ms pulse widths and 2 Ω and 50 Ω line impedance, respectively. This is a relatively small amount of energy when compared to the forward surge current at the load dump test condition.

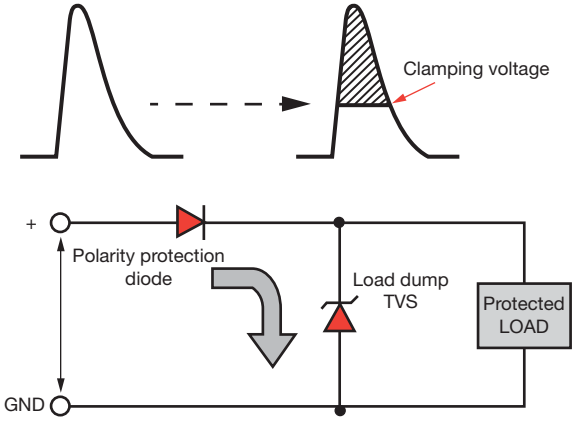

Fig. 6 - Load Dump Suppression

Load dump suppression is simulated by tests such as ISO-16750-2 test A and B, JASO standard type A and D, and others.

TABLE 4: ISO-16750-2, TEST PULSE A

PARAMETER	TYPE OF SYSTEM		MINIMUM TEST REQUIREMENTS
	12 V	24 V	
U_sa (V)	79 to 101	151 to 202	10 pulses at intervals of 1 minute
R_ia (Ω)	0.5 to 4	1 to 8	
t_d (ms)	40 to 400	100 to 350	
t_r (ms)	10/0/-5	10/0/-5	

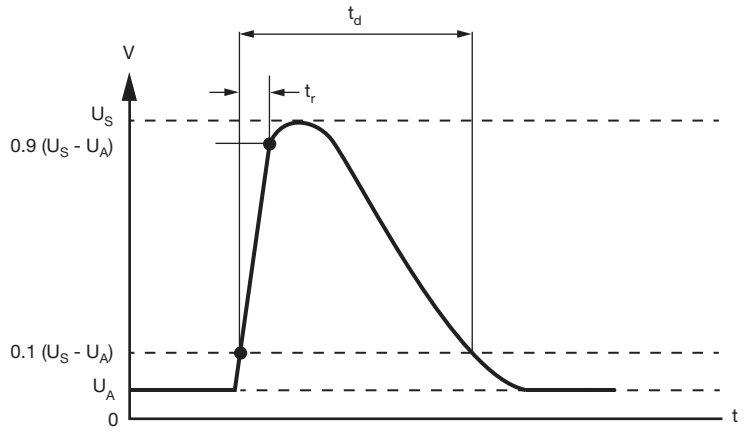

Fig. 7 - ISO-16750-2, Test Pulse A

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TABLE 5: ISO-16750-2, TEST PULSE B			
PARAMETER	TYPE OF SYSTEM		MINIMUM TEST REQUIREMENTS
	12 V	24 V	
$U_s a$ (V)	79 to 101	151 to 202	10 pulses at intervals of 1 minute
U_s (V)	35	65	
$R_i a$ (Ω)	0.5 to 4	1 to 8	
t_d (ms)	40 to 400	100 to 350	
t_r (ms)	10/0/-5	10/0/-5	

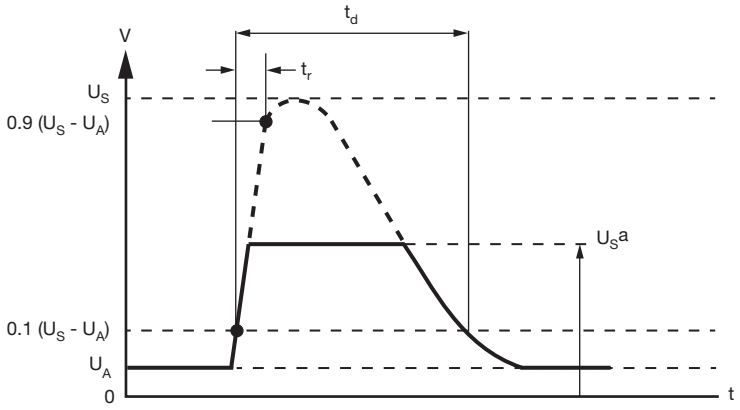

Fig. 8 - ISO-16750-2, Test Pulse B

TABLE 6: JASO D001-94, TYPE A AND D							
CLASSIFICATION	TYPE OF TEST		V_p (V)	t_d (µs)	f (Hz)	R_i (Ω)	NUMBER OF PULSES
12 V system	Type	A-1	70	200 000	-	0.8	1
		A-2	110	2.5	1/30	0.4	10
24 V system		D-1	110	400 000	-	1.5	1
		D-2	170	2.5	1/30	0.9	10

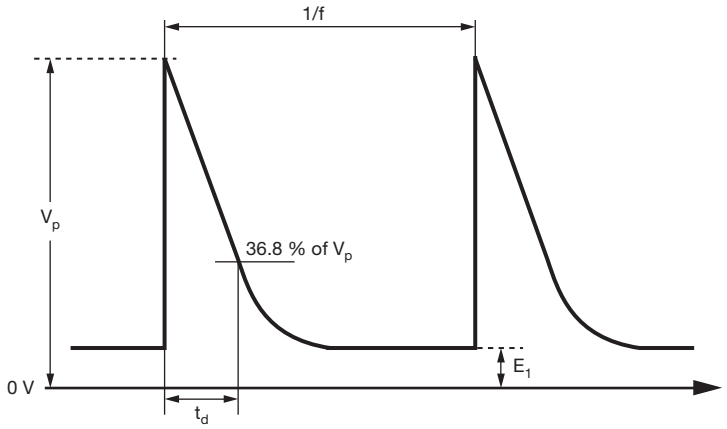

Fig. 9 - JASO D001-94, Type A and D

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In this situation, high surge current is passing through the polarity protection diode, and it requires a high enough forward surge capability to avoid failure. Estimating the surge current value in load dump suppression tests can be accomplished with the equation:

$I_{peak} = (V_{peak} - V_{Fd} - V_{clamping})/(R_i + R_{zd})$

V_{peak}: Surge voltage

$V_{clamping}$: Clamping voltage

V_{Fd}: Forward voltage drop of polarity protection diode

R_i: Line impedance

R_{zd}: Resistance of clamping device

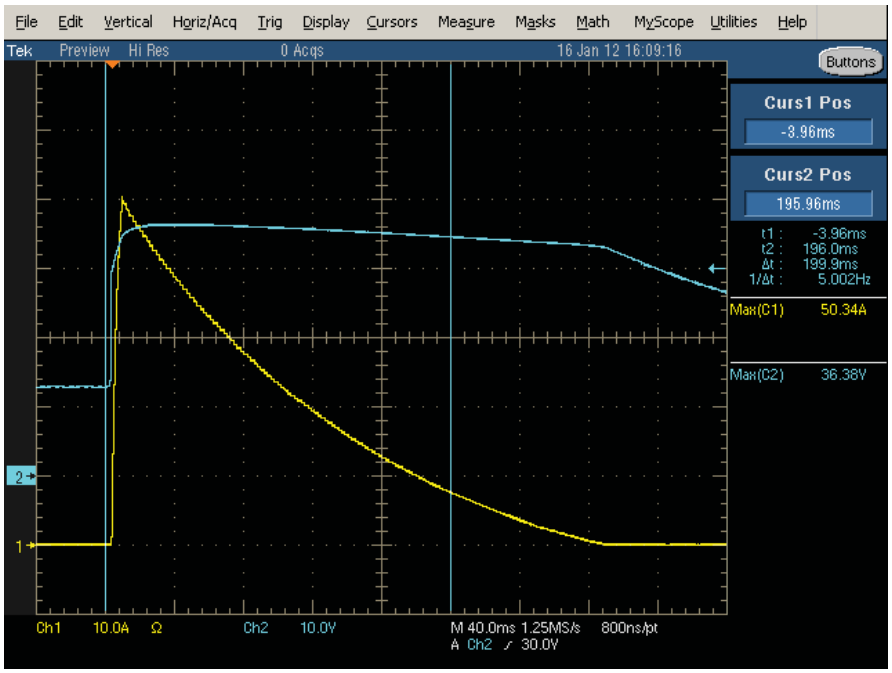

Fig. 10 - With the Applied Condition of 101 V U_s, 12 V U_B, and 1.25 Ω Line Impedance, as Specified by ISO-16750-2 test A, the Peak Current is 51.3 A and the Actual Clamped Current is 50.3 A.

For a detailed explanation of load dump protection, please refer to www.vishay.com/doc?88490

ESD

ESD influences the operating stability and lifetime reliability of electronic modules in vehicles.
ISO-10605 and JASO standard 5.8 specify testing conditions for this parameter.

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TABLE 7: ISO-10605: 2001 B.4.2, TEST SEVERITY LEVELS FOR ELECTRONIC MODULES (POWER-UP TEST)						
TYPE OF DISCHARGE	SEVERITY LEVEL					MINIMUM NUMBER OF DISCHARGES (1)
	SELECTED LEVEL	I	II	II	IV	
Direct discharge	(2)	± 4	± 6	± 7	± 8	3
Air discharge	(2)	± 4	± 8	± 14	± 15	

Notes

(1) Minimum delay between discharges is 5 s

(2) Values to be agreed between vehicle manufacturer and supplier

TABLE 8: JASO D001-94 AUTOMOBILE STANDARD					
TYPE OF TEST		TEST CONDITIONS			
		TEST VOLTAGE (kV)	IMPRESSING CYCLE TIMES	NUMBER OF IMPRESSIONS	LOCATION OF IMPRESSIONS
Type A	A-1	± 0.5	1 s or more	3 times or more	Input and output terminals
	A-2	± 1			
Type B	B-1	± 1			Operating portion
	B-2	± 5			
Type C	C-1	± 5			
	C-2	± 10			
	C-3	± 15			

Non-Repetitive Avalanche Energy (E_{AS})

This non-repetitive avalanche energy of a diode specifies the maximum energy it can absorb in the reverse bias state to protect circuits from inductive kick back transients from motors and solenoids, or induced high reverse voltages. There is no automotive standard for this specification.

Temperature Conditions for Automotive Electronics and Components

The JASO specifies the operating temperature range for automotive electronics as - 40 °C to + 100 °C based on their location, such as the trunk, engine, or other places.

TABLE 9: SETTING TEMPERATURES FOR TESTING	
CLASSIFICATION OF EQUIPMENT	SETTING TEMPERATURES (°C)
Class 1	- 30, - 5, 25, 65, 80
Class 2	- 30, - 5, 25, 65, 80
Class 3	- 30, - 5, 25, 65, 100 (125) (1)
Class 4	As agreed between the persons concerned

Note

(1) The (125) of Class 3 is carried out according to the necessary conditions

Equipment is classified as follows:

- Class 1: Installed in the vehicle compartment and the trunk room (other than Class 4)
- Class 2: Installed outside the vehicle (other than Class 4)
- Class 3: Installed inside the engine room (other than Class 4)
- Class 4: Installed at or near the high-temperature portion or other special portion

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VISHAY RECTIFIERS FOR POWER LINE POLARITY PROTECTION

TABLE 10: VISHAY'S HIGH CURRENT DENSITY SURFACE MOUNT ESD CAPABILITY RECTIFIERS

SERIES	V_{RRM} (V)	I_F (A)	I_{FSM} (A)	V_F (V) AT I_F (A)		PACKAGE
MSE1P	100 to 600	1.0	20	0.925	1.0	MicroSMP
SE10P		1.0	25	0.860	1.0	DO-220AA (SMP)
SE15P		1.5	30	0.868	1.5	DO-220AA (SMP)

Vishay's ESD capability rectifiers offer low forward voltage drop and meet ESD test levels as outlined in the following table.

TABLE 11: ESD IMMUNITY STANDARDS
(T_A = 25 °C unless otherwise noted)

STANDARD	TEST TYPE	TEST CONDITIONS	SYMBOL	CLASS	VALUE
AEC-Q101-001	Human body model (contact mode)	C = 100 pF, R = 1.5 Ω	V_C	H3B	> 8 kV
AEC-Q101-002	Machine model (contact mode)	C = 200 pF, R = 0 Ω		M4	> 400 kV
JESD22-A114	Human body model (contact mode)	C = 150 pF, R = 1.5 Ω		3B	> 8 kV
JESD22-A114	Machine model (contact mode)	C = 200 pF, R = 0 Ω		C	> 400 kV
IEC 61000-4-2 (2)	Human body model (contact mode)	C = 150 pF, R = 150 Ω		4	> 8 kV
	Human body model (air -discharge mode) (1)	C = 150 pF, R = 150 Ω		4	> 15 kV

Notes

(1) Immunity to IEC 61000-4-2 air discharge mode has a typical performance > 30 kV

(2) System ESD standard

Vishay's avalanche rectifiers offer the low forward voltage drop of common rectifiers, while providing the avalanche capability to protect circuits from induced transient voltages through the power line, inductive kick back transient voltage from motors and solenoids, and induced transient voltages from outside the power line.

TABLE 12: VISHAY'S SURFACE MOUNT AVALANCHE RECTIFIERS

SERIES	V_{RRM} (V)	I_F (A)	I_{FSM} (A)	V_F (V) AT I_F (A)		E_{AS} (mJ)	PACKAGE
AS1P	200 to 1000	1.5	30	0.89	1.5	20	DO-220A
BYG10	200 to 1600	1.5	30	1.15	1.5	20	DO-214AC (SMA)
AS3BJ	600	3.0	90	0.88	3.0	30	DO-214AA (SMB)
AS3P	200 to 1000	3.0	70	0.90	3.0	30	TO-277A
AS4P	200 to 1000	4.0	100	0.92	4.0	30	TO-277A

Avalanche rectifiers are designed to protect against avalanche breakdown, which is caused by ionization created by electron-hole pairs. This is different than Zener breakdown, which results from quantum mechanical tunneling of carriers through the band-gap in highly doped p-n junctions.

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References

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IEC 61000-4-2: 1995: Electromagnetic compatibility (EMC) - Part 4: Testing and measurement techniques; Section 2: Electrostatic discharge immunity test

ISO-10605: 2001: Road vehicles - Test methods for electrical disturbances from electrostatic discharge

ISO-16750-2: 2010: Road vehicles - Environmental conditions and testing for electrical and electronic equipment

ISO-7637-2: 2010: Road vehicles - Electrical disturbance by conduction and coupling – Part 2: Electrical transient conduction along supply lines only

JASO D001-94: Japanese automobile standard - General rules of environmental testing methods for automotive electronic equipment

IEC 61000-4-2: 1995 Electromagnetic compatibility (EMC) - Part 4: Testing and measurement techniques - Section 2: Electrostatic discharge immunity tes