Measuring Power MOSFET Characteristics

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This application note describes methods for measuring Power MOSFET characteristics, both with a curve tracer and with special-purpose test circuits.

APPLICATION NOTE

Measuring Power MOSFET Characteristics

TOPICS COVERED:

- Converting the nomenclature from bipolars to MOSFETs
- P-channel Power MOSFETs
- Initial settings
- Breakdown
- Drain leakage
- Gate threshold
- Gate leakage
- Transconductance
- On-resistance
- Diode drop
- Characteristics in synchronous rectification
- Transfer characteristics
- Measurements without a curve tracer
- Device capacitances
- Switching times
- Gate charge
- Reverse recovery
- A fixture to speed-up testing time
- Related topics

1. GENERAL

Curve tracers have generally been designed for making measurements on bipolar transistors. While Power MOSFETs can betested satisfactorily on most curve tracers, the controls of these instruments are generally labeled with reference to bipolar transistors, and the procedure to follow in the case of MOSFETs is not immediately obvious. This application note describes methods for measuring Power MOSFET characteristics, both with a curve tracer and with special-purpose test circuits. Testing Power MOSFETs on a curve tracer is a simple matter, provided the broad correspondence between bipolar transistor and Power MOSFET features are borne in mind. Table 1 matches some features of Power MOSFETs with their bipolar counterparts. The Power MOSFET used in all the examples is the IRF630. The controlsettings given in the examples are those suitable for the IRF630. The user must modify these values appropriately when testing adifferent device. The IRF630 was selected since it is a typical mid-range device with a voltage rating of 200 V and acontinuous current rating of 9 A (with T_C = 25 °C). For measurements with currents above 20 A, or for pulsed tests notcontrolled by the gate, the Tektronix 176 Pulsed High Current Fixture must be used instead of the standard test fixture.

The IRF630 is an n-channel device. For a p-channel device, all the test procedures are the same except that the position of the Polarity Selector Switch must be reversed - that is, for p-channel devices, it must be in the PNP position.

The curve tracer used as an example in this application note is a Tektronix 576, since this instrument is in widespread use. However, the principles involved apply equally well to other makes and models. Figure 1 shows the layout of the controls of the Tektronix 576 curve tracer, with major controls identified by the names used in this application note. Throughout this applicationnote, when controls are referred to, the name of the control is printed in capitals. For all tests, when the power is on, the initialstate of the curve tracer is assumed to be as follows:

- **Left/right** switch in “off” position
- **Variable collector supply** at zero
- **Display** not inverted
- **Display offset** set at zero
- **Step/offset polarity** button out (not inverted)
- **Vert./horiz. display magnifier** set at **norm (off)**
- The **rep** button of the **step family** selector should be **in**
- The **aid** button of the **offset** selector should be **in**
- The **norm** button of the **rate selector** should be **in**

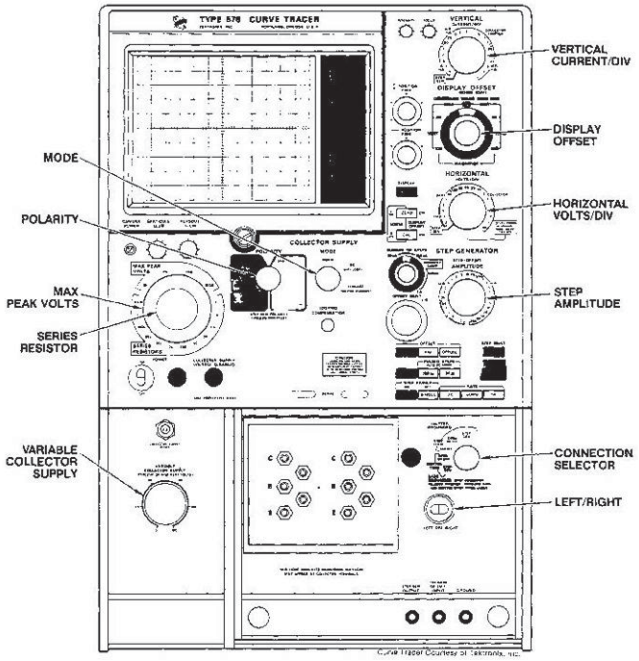

Fig. 1 - Location of controls in a 576 curve tracer

The accuracy of all tests is predicated on the correct use of the Kelvin connections, as indicated in the instructions for the curve tracer. This is particularly important for power semiconductors, as inductive and resistive drops across sockets and wiring are significant.

Some tests require the use of high voltages. After the device is mounted in the test fixture as described for each test, the test fixture safety cover should be closed and the curve

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tracer manufacturer's safety warnings heeded. The exposed metal parts of many Power MOSFETs (for example, the tab of TO-220 devices) are connected to the drain and are therefore at the potential of the collector supply.

As with any semiconductor device, some of the characteristics of Power MOSFETs are temperature dependent. For tests in which there is significant heating of the Power MOSFET, a low repetition rate should be used. For tests involving a slow transition through the linear region, a damping resistor of at least 10 Ω should be connected in series with the gate, close to the gate lead to prevent oscillations. If frequent testing of MOS-gated devices is expected, the use of a test fixture that plugs directly into the curve tracer would save a significant amount time. Such a fixture is descibed in Section 12. MOS-gated transistors are static sensitive. Wrist straps, grounding mats and other ESD precautions must be followed, as indicated in INT-955.

2. BV_{DSS}

This is the drain-source breakdown voltage (with V_{GS} = 0). BV_{DSS} should be greater than or equal to the rated voltage of the device, at the specified leakage current.

1. Connect the device as follows: drain to "C", gate to "B", source to "E".
2. Set the **max. peak V** to 350 V.
3. Set the **series resistor** to limit the avalanche current to a safe value (i.e., tens of mA). A suitable value in this case would be 14 kΩ.
4. Set the **polarity** switch to **NPN**.
5. The **mode** control should be set to **norm**.
6. **Horizontal V/div.** should be set at 50 V/div. on the "collector" range.
7. **Vertical current/div.** should be set at 50 µA/div.
8. On the plug-in fixture, the **connection selector** should be set to **"short"** in the **"emitter grounded"** sector. This action grounds the gate and disables the step generator.
9. Connect the device using the **left/right** switch. Increase the collector supply voltage using the **variable collector supply** control until the current (as indicated by the trace on the screen) reaches 250 µA. (see figure 2.) Read BV_{DSS} from the screen.

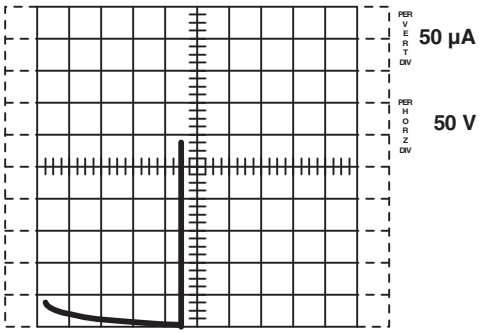

Fig. 2 - Drain-source breakdown voltage

3. I_{DSS}

This is the drain current for a drain-source voltage of 100 % of rated voltage, with V_{GS} = 0. This measurement is made in the same manner as BV_{DSS}, except that:

1. The **mode** switch is set to **"leakage"**.
2. Connect the device using the **left/right** switch and adjust the collector supply voltage to the rated voltage of the Power MOSFET (200 V for the IRF630). Read the value of I_{DSS} from the display (see figure 3). The vertical sensitivity may need altering to obtain an appropriately sized display. Often I_{DSS} will be in the nA range and the current observed will be capacitor currents due to minute variations in collector supply voltage.

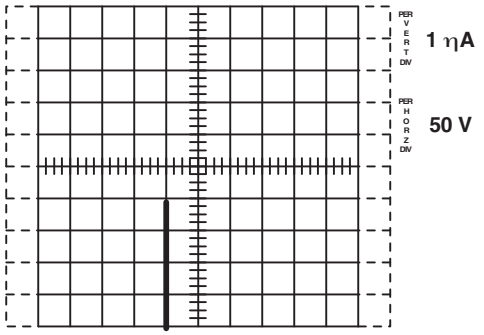

Fig. 3 - Drain-source breakdown voltage

4. $V_{GS(th)}$

This is the gate-source voltage which produces 250 µA of drain current (V_{DS} = V_{GS}). At this gate-source voltage the device enters the active region. In circuits where devices are connected in parallel, switching losses can be minimized by using device swith closely matched threshold voltages. This test requires the gate to be connected to the drain and conducted as follows:

1. Connect the device as follows: source to "E", gate to "B", drain to "C". This connection arrangement may require the construction of a special test fixture. Bending of the device leads can cause mechanical stress which results in the failure of the device.

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2. Set the **max. peak V** to 15 V.
3. Set the **series resistor** to 0.3 Ω.
4. Set **polarity** to **PNP**. This causes the drain (collector) terminal to be negative with respect to the source (emitter) terminal.
5. Set the **mode control** to **norm**.
6. Set the **vertical current/div.** to 50 µA/div.
7. Set the **horizontal V/div.** to 500 mV/div.
8. Set the **connection selector** to **"short"** in the **"emitter grounded"** sector.
9. **Display** should be inverted.
10. Connect the device using the **left/right** switch. Increase the **variable collector voltage** until the drain current reaches 250 µA as indicated by the trace on the screen. Read the voltage on the horizontal center line (since this line corresponds to I_D = 250 µA) (see figure 4).

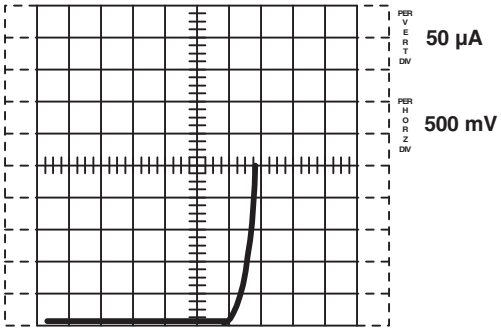

Fig. 4 - Gate-source threshold voltage

5. I_{GSS}

This is the gate-source leakage current with the drain connected to the source. An excessive amount of gate leakage current indicates gate oxide damage.

1. The device is connected as follows: gate to "C", drain to "B", source to "E". This is not the usual connection sequence, and a special test fixture will be required if bending of the leads is to be avoided.
2. Set the **max. peak V** to 75 V.
3. Set the **series resistor** to a low value (for example., 6.5 Ω).
4. Set **polarity** to **NPN**.
5. Set the **mode** switch to **leakage**.
6. Set the **connection selector** to the **"short"** position in the **"emitter grounded"** sector.
7. **Horizontal V/div.** should be set at 5 V/div.
8. **Vertical current/div.** should be set to an appropriately low range.
9. Connect the device using the **left/right** switch. Increase the collector supply voltage using the **variable collector supply** control, but do not exceed 20 V, the maximum allowable gate voltage. It may be necessary to adjust the vertical sensitivity. Read the leakage current from the display (see figure 5). In many cases, the leakage current will be inthe nA range, in which case the trace will be dominated by currents which flow through the device capacitance as aresult of minute fluctuations in the collector supply voltage.
10. The above procedure is for determining gate leakage current with a positive gate voltage. To make the same measurement using a negative voltage, reduce the **variable collector supply** voltage to zero, change the **polarity** switch to the **PNP** position, and reapply the voltage (see figure 6). The trace will take time to settle because of the gate-source capacitance.

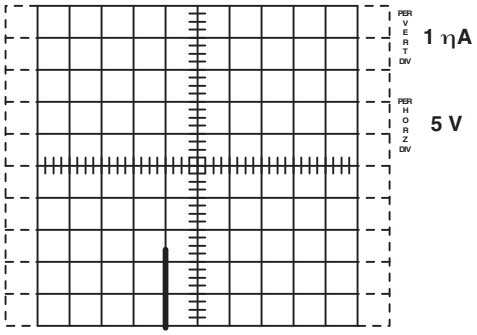

Fig. 5 - Gate-source threshold voltage

6. g_{fs}

This is the forward transconductance of the device at a specified value of I_D. g_{fs} represents the signal gain (drain current divided by gate voltage) in the linear region. This parameter should be measured with a small AC superimposed on a gate bias and the curve tracer is not the appropriate tool for this measurement. Even with specific test equipment, as indicated in section 11, the DC bias tends to overheat the MOSFET very rapidly and care should be exercised to insure that the pulse is suitably short.

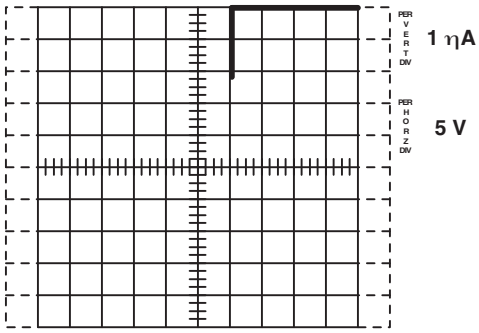

Fig. 6 - Gate-source leakage current at - 20 V

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7. $R_{DS(ON)}$

This is the drain-source resistance at 25 °C with V_{GS} = 10 V. Since $R_{DS(on)}$ is temperature-dependent, it is important to minimize heating of the junction during the test. A pulse test is therefore used to measure this parameter. The test is set up in the following manner:

1. Connect the device as follows: gate to “B”, drain to “C”, source to “E”.
2. Set the **max. peak V** to 15 V.
3. Set the **series resistor** to 0.3 Ω.
4. The **polarity** switch should be set to **NPN**.
5. The **mode** switch should be set to **“norm”**.
6. Set the **step amplitude** to 1 V.
7. Set **number of steps** to 10.
8. Set **offset mult** to 0.
9. The **current limit** should be set to 500 mA.
10. The **step multiplier** button should be **out** - that is, 0.1X not selected.
11. On the **pulsed steps** selector, the 80 µs button should be **in** (or the 300 µs, if the 80 is not available).
12. On the **rate** selector, the 0.5X button should be **in**.
13. Set **vertical current/div.** at 1 A/div. (IRF630). This scales hould be chosen according to the on-resistance of the device being tested.
14. Set the **connection selector** to the **“step gen”** position in the **“emitter grounded”** sector.
15. Connect the device using the **left/right** switch and raise the **variable collector supply** voltage until the desired value of drain current is obtained. $R_{DS(on)}$ is obtained from the trace by reading the peak values of current and voltage (see figures 7 and 8).

$R_{DS(on)} = V_{DS}/I_D$.

Logic level devices would have different settings for 6, 7, and 8 so that the on-resistance is measured at the specified gate voltage.

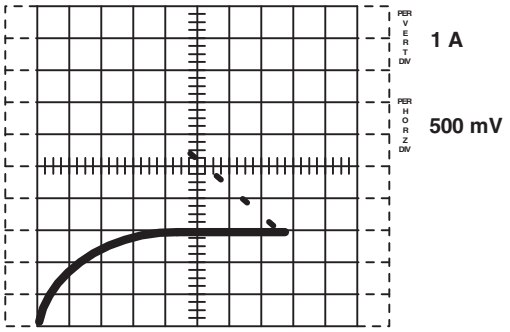

Fig. 7 - Drain-source resistance, pulsed mode

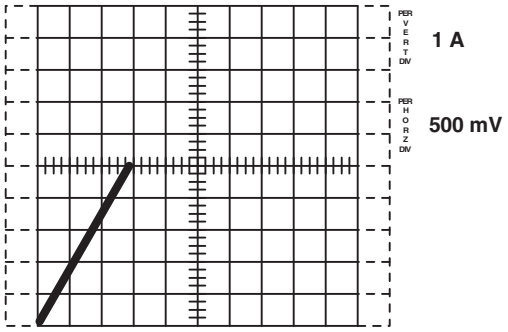

Fig. 8 - Drain-source resistance

8. V_{SD}

This is the source-drain voltage at rated current with V_{GS} = 0. It is the forward voltage drop of the body-drain diode when carrying rated current. If pulsed mode testing is required, use high current test fixture.

1. Connect the device as follows: gate to “B”, drain to “C”, source to “E”.
2. Set the **max. peak V** to 15 V.
3. Set the **series resistor** at 1.4 Ω or a value sufficiently low that rated current can be obtained.
4. Set **polarity** to **PNP**.
5. Set the **mode** switch to **“norm”**.
6. The 80 µs button of the **pulsed steps** selector should be **in** (or the 300 µs, if the 80 is not available).
7. The **connection selector** should be set to the **“short”** position in the **“emitter grounded”** sector.
8. **Horizontal V/div.** should be on 200 mV/div.
9. **Vertical current div.** should be on 1 A/div.
10. The **display** button should be set to invert.
11. The device is connected using the **left/right** switch. Increase the **variable collector supply** voltage until rated current is reached (9 A for the IRF630). Read V_{SD} from the trace (see figure 9).

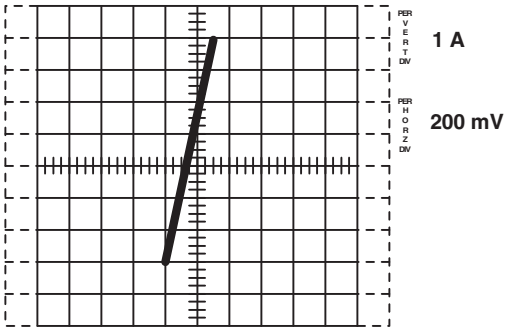

Fig. 9 - Source-drain voltage (diode)

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9. COMPOSITE CHARACTERISTICS

The forward and reverse characteristics of the Power MOSFET may be viewed at the same time. This display can beused to obtain an appreciation of the Power MOSFET's behavior in applications in which current flows in the channelin either direction. such as synchronous rectifiers and analog waveform switching. The procedure is the same as for on-resistance except that:

1. **Offset** is set to zero.
2. The **polarity** control is set at **"AC"**.
3. The device is connected using the **left/right** switch. The **variable collector supply** voltage is increased to obtain the required peak value of I_D. Beware of device heating. Figure 10 shows the trace obtained with the IRF630. To obtain the reverse characteristics of the diode alone, invert the step polarity. The FET is inoperative, and the display will resemble that shown in figure 11. The step polarity should also be inverted to obtain the composite characteristics of p-channel devices.

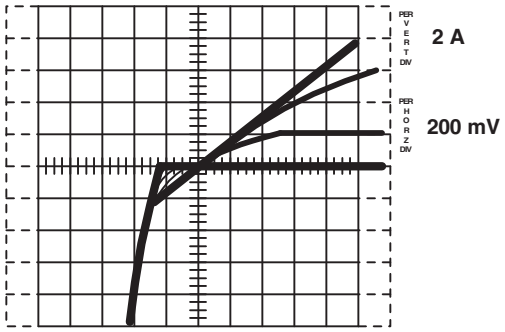

Fig. 10 - Operation in first and third quadrant (synchronous rectification)

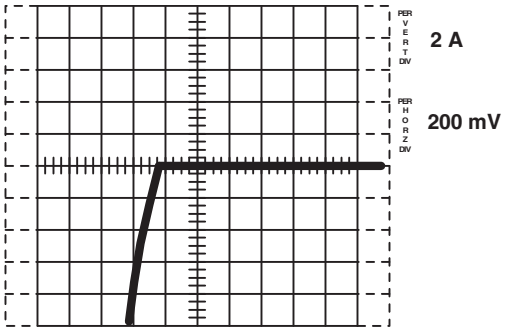

Fig. 11 - Operation in first and third quadrant without gate drive

10. TRANSFER CHARACTERISTICS

The transfer characteristic curve of I_D versus V_{GS} may be displayed usingthe pulse mode. The test is set up in the same manner as the on-resistance test, except for the following:

1. **Offset multiply** should be set at zero.
2. Set **horizontal V/div.** on **"step gen"**.
3. The 300 µs button of the **pulsed step selector** should be **in**.
4. Increase the **variable collector supply** voltage to obtain the trace shown in figure 12. The transfer characteristic is outlined by the displayed points.

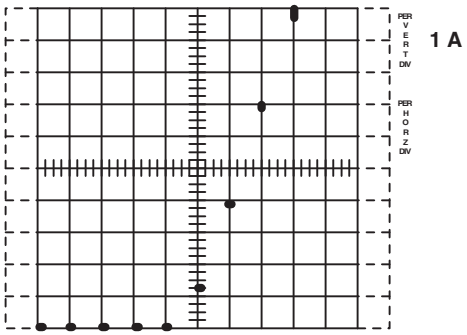

Fig. 12 - Transfer characteristic (I_D vs. V_{GS})

11. MEASUREMENT OF POWER MOSFET CHARACTERISTICS WITHOUT A CURVE TRACER

Power MOSFET parameters can be measured usingstandard laboratory equipment. Test circuits and procedures fordoing this are described in the following sections, with the IRF630 used as an example. The test arrangement should be variedappropriately for other devices.

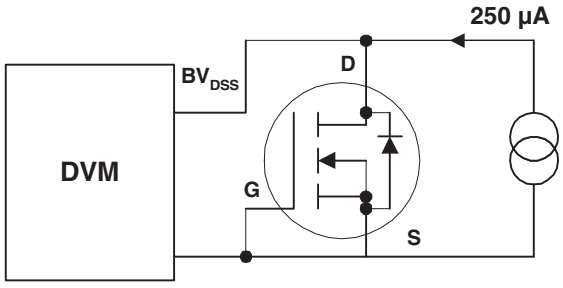

Fig. 13 - Test circuit for BV_{DSS}

BV_{DSS}, Drain-Source Breakdown Voltage

The test circuit is shown in figure 13. The current source will typically consist of a power supply with an output voltage capability of about 3 time BV_{DSS} in series with a current defining resistor of the appropriate value. When testing high voltage Power MOSFETs it may not be practical or safe to use a supply of 3 times BV_{DSS}. In such cases, another type of constant current source may be used.

$V_{GS(th)}$, Threshold Voltage

The test circuit is shown in figure 14. The 1 kΩ gate resistor is required to suppress potentially destructive oscillations at the gate. The current source may be derived from a voltage

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source equal to the gate voltage rating of the Power MOSFET and a series resistor.

$V_{DS(on)}$, On-Resistance

The test circuit is shown in figure 15. The pulse width should be 300 µs at a duty cycle of less than 2 %.The value quoted is at a junction temperature of 25 °C. $R_{DS(on)}$ is calculated by dividing $V_{DS(on)}$ by I_D. Connect the ground of the gate supply as close to the source lead as possible.

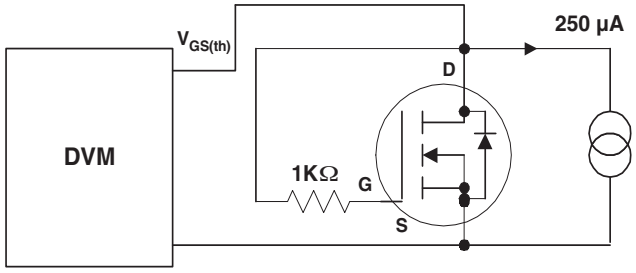

Fig. 14 - Test circuit for BV_{DSS}

g_{fs}, Transconductance

Connect a 50 V power supply between the device drain and source, as shown in figure 16. Use a current probe to measure I_D. A signal generator operating at low duty cycle to prevent heating of the device, is used to obtain 80 µs pulses of the required voltage (V_{GS}) to obtain the following currents: 0.015 x I_D , 0.05 x I_D , 0.15 x I_D , 0.5 x I_D , and 1.5 x I_D where I_D is the rated value at T_C = 25 °C. Plot a graph of V_{GS} vs. I_D.The transconductance is equal to the slope of.

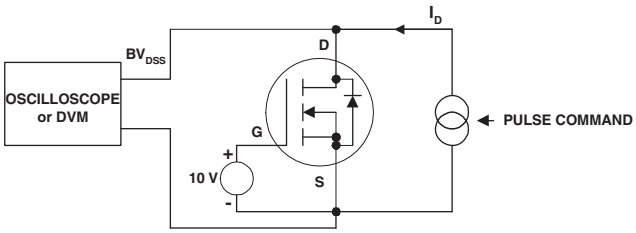

Fig. 15 - Test circuit for drain on-state voltage

C_{iss}, C_{oss}, and C_{rss}. Output, input and reverse transfer capacitances

A 1 MHz capacitance bridge is used for all these tests. The capacitance to be measured is connected in series with a capacitance of known value to provide dc isolation. If C_u is the unknown capacitance, C_k is the known capacitance, and C_m is the measured capacitance, then C_u can be calculated as follows:

$$C_u = \frac{C_k \times C_m}{C_k - C_m} \quad (1)$$

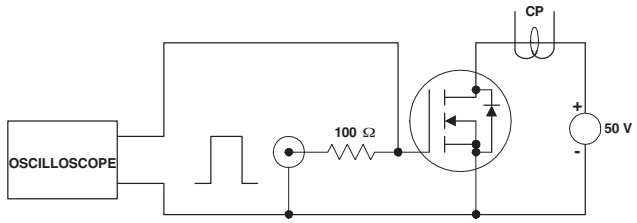

Fig. 16 - Test circuit for transconductance

Figures 17, 18 and 19 show the circuit connections for the three capacitances that characterize Power MOSFETs.

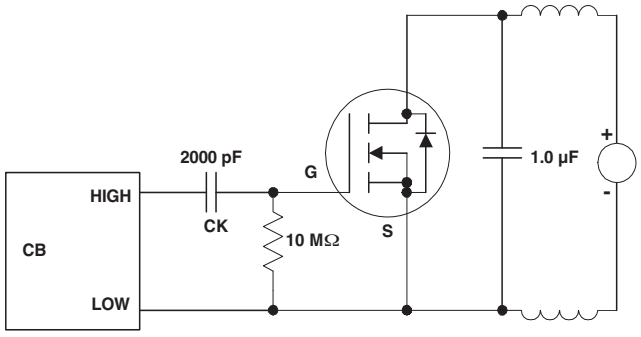

Fig. 17 - Test circuit for input capacitance

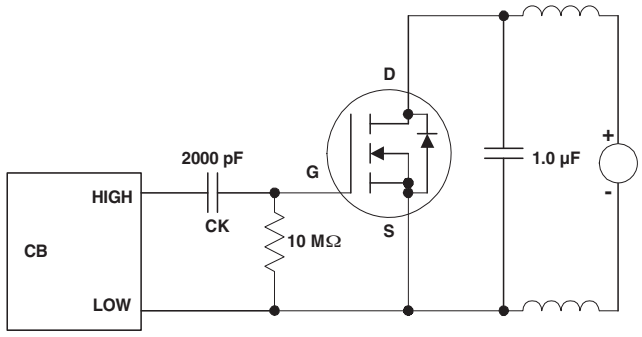

Fig. 18 - Test circuit for output capacitance

Turn-on Delay Time, Rise Time, Turn-Off Delay Time, Fall Time

Data sheet value are for a resistive load, as shown in figure 20, as well as individual data sheets. The gate pulses should be just long enough to achieve complete turn-on, with a duty cycle of the order of 0.1 %.

The series resistor is as specifyed in the datasheet. The definitions of rise, fall and delay times are given in figure 21. Power MOSFETs can switch in ns. Unless the test circuit is laid-out with RF techniques, the measurements will be totally unreliable. Switching time measurements frequently amount to a characterization of the test circuit, rather than the device under test. Gate charge provides a better indication of the switching capability of Power MOSFETs.

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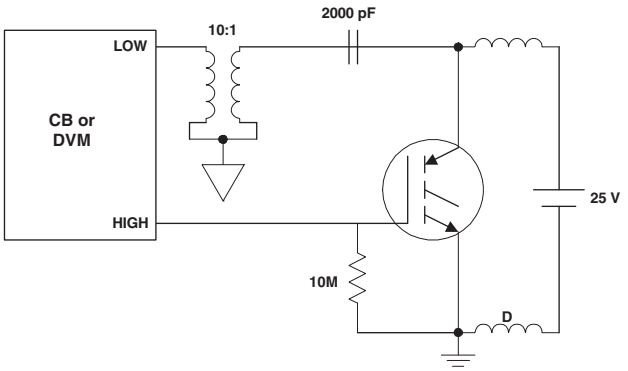

Fig. 19 - Test circuit for transfer capacitance

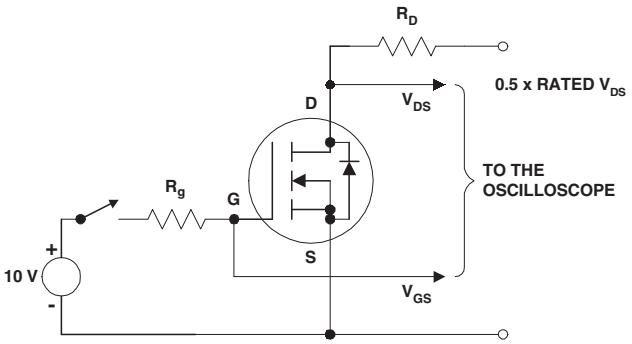

Fig. 20 - Test circuit for switching times

Q_g, Q_{gs}, Q_{gd} Total Gate charge, Gate-Source charge, Gate-Drain charge

The total gate charge has two components: the gate-source charge and the gate-drain charge (often called the Miller charge). INT-944 gives more details on this test. Figures 22 and 23 show the testcircuit and waveforms. From the relationship Q = $\int$i, the following results are obtained:

$Q_g = (t_3 - t_0)\ i_g$,
$Q_{gd} = (t_2 - t_1)\ i_g$,
$Q_{gs} = Q_g - Q_{gd}$

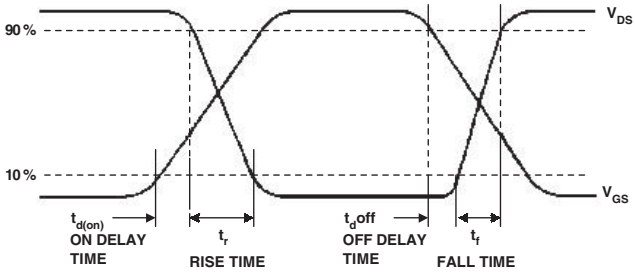

Fig. 21 - Switching time waveforms

V_{SD} Body-Drain Diode Voltage Drop

The current source may consist or a voltagesource and a series resistor, as shown in figure 24. The voltage should be applied in short pulses (less than 300 µs) with a low duty cycle (less than 2 %).

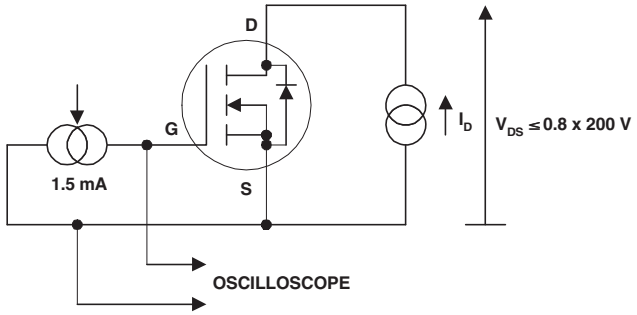

Fig. 22

t_{rr}, Q_{rr} body-drain diode reverse recovery time and reverse recovery charge

Several test circuits are commonly used to characterize these parameters. Some have been qualified by JEDEC. The datasheet indicates the test method used for the specific device.

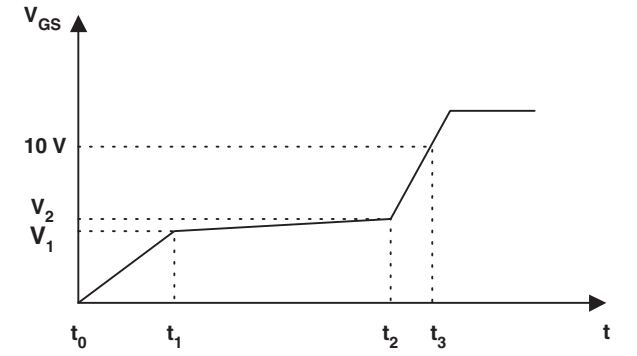

Fig. 23 - Gate charge waveforms

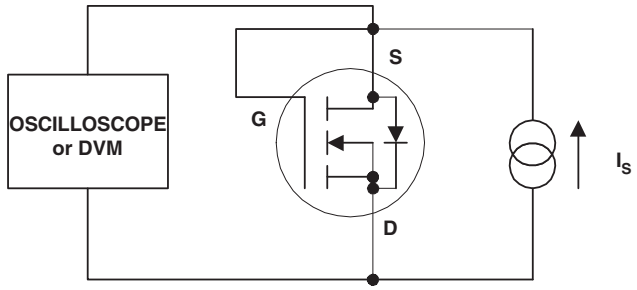

Fig. 24 - Test circuit MOSFET diode drop

12. A FIXTURE TO SPEED-UP TESTING TIME

The most commonly tested parameters in a MOS-gated transistor are gate-source leakage (I_{GSS}), drain-source resistance ($R_{DS(on)}$), breakdown voltage (BV_{DSS}), drain current (I_{DSS}), source-drain voltage (V_{SD}), threshold ($V_{GS(th)}$), and soon. These tests can begreatly simplifyed with the fixture shown in figure 25.

APPLICATION NOTE

Measuring Power MOSFET Characteristics

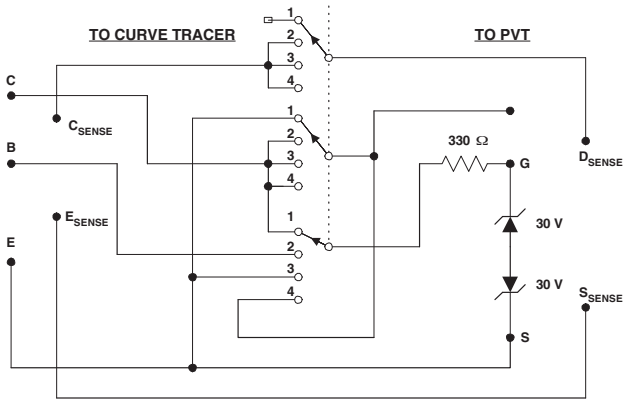

Fig. 25 - Test fixture for Power MOSFET test

Position	Measurement	Comment
1	I_{GSS}	C sense disconnected, Drain Source S/C connected, Collector Voltage applied to gate via 330 Ω resistor. Note: Gate protected by back to back 30 V zeners.
2	$R_{DS(on)}$	Collector Voltage applied to Drain Based Voltage applied to Gate via 330 Ω resistor.
3	$BV_{DSS}/I_{DSS}/V_{DS}$	Collector Voltage applied to Drain, Gate Source S/C connected via 330 Ω resistor.
4	$V_{GS(th)}$	Collector Voltage applied to Drain, Gate Drain S/C connected via 330 Ω resistor.

Related topics:

- Parameter definition in IGBTs
- Gate Charge
- Thermal characteristics
- ESD sensitivity
- ESD test methods

APPLICATION NOTE