

Vishay Siliconix

E Series Power MOSFET

DESCRIPTION

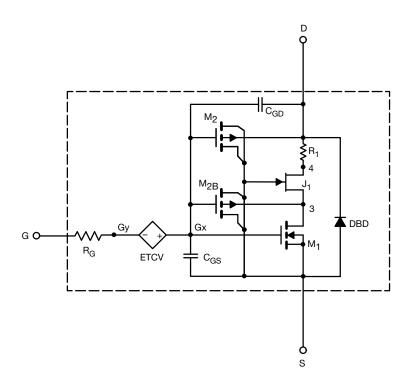
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

CHARACTERISTICS

- N-channel vertical DMOS
- · Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- · Model the gate charge

SUBCIRCUIT MODEL SCHEMATIC



Note

• This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.





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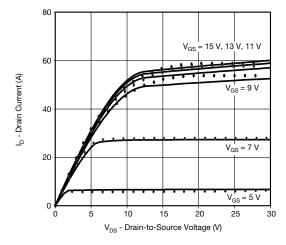
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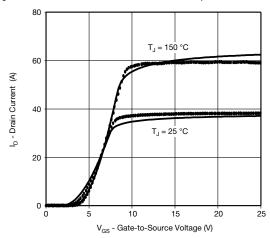
| SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | |
|---|---------------------|--|----------------|------------------|------|
| PARAMETER | SYMBOL | TEST CONDITIONS | SIMULATED DATA | MEASURED DATA | UNIT |
| Static | | | | | |
| Gate-Source Threshold Voltage | V _{GS(th)} | $V_{DS} = V_{GS}, I_D = 250 \mu A$ | 2.3 | - | V |
| Drain-Source On-State Resistance | R _{DS(on)} | $V_{GS} = 10 \text{ V}, I_D = 11 \text{ A}$ | 0.15 | 0.15 | Ω |
| Forward Transconductance | 9 _{fs} | $V_{DS} = 8 \text{ V}, I_{D} = 5 \text{ A}$ | 6 | 6.4 | S |
| Dynamic | | | | | |
| Input Capacitance | C _{iss} | V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz | 2222 | 1920 | pF |
| Output Capacitance | Coss | | 208 | 90 | |
| Reverse Transfer Capacitance | C _{rss} | | 16 | 6 | |
| Total Gate Charge | Q_g | V _{DS} = 480 V, V _{GS} = 10 V, I _D = 11 A | 57 | 57 | nC |
| Gate-Source Charge | Q _{gs} | | 14 | 14 | |
| Gate-Drain Charge | Q_{gd} | | 26 | 26 | |
| Drain-Source Body Diode Characteristics | | | | | |
| Diode Forward Voltage | V_{SD} | $T_J = 25 ^{\circ}\text{C}, I_S = 11 \text{A}, V_{GS} = 0 \text{V}$ | 0.83 | - | V |
| Reverse Recovery Time | t _{rr} | $T_J = 25 ^{\circ}\text{C}, I_F = I_S = 11 \text{A},$ $dI/dt = 100 \text{A/}\mu\text{s}, V_R = 25 \text{V}$ | 340 | 344 | ns |
| Reverse Recovery Charge | Q_{rr} | | 5.6 | 5.3 | μC |

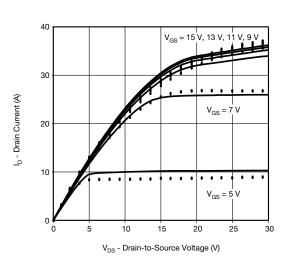
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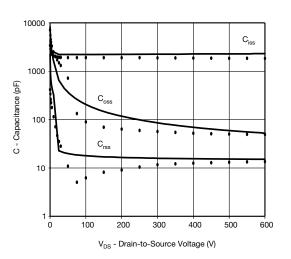
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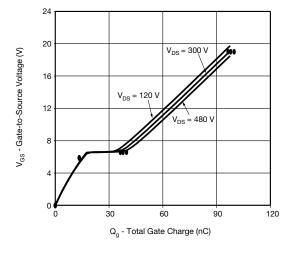
COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25$ °C, unless otherwise noted)

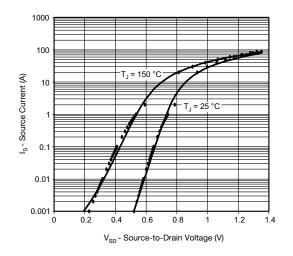












Note

Dots and squares represent measured data.
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