## SPICE Device Model SiHP22N60E



**Vishay Siliconix** 

# **E Series Power MOSFET**

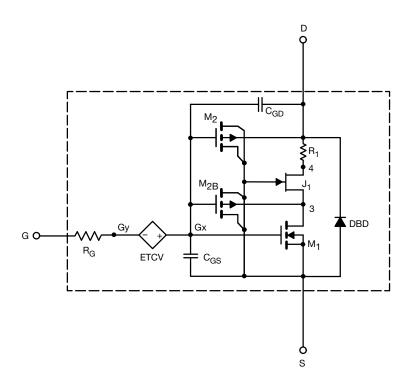
#### DESCRIPTION

The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over 25 °C to 150 °C temperature ranges under the pulsed 0 V to 15 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}\xspace$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### **CHARACTERISTICS**

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- · Apply for both linear and switching application
- Accurate over 25 °C to 150 °C temperature range
- · Model the gate charge



### SUBCIRCUIT MODEL SCHEMATIC

#### Note

This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



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<b>SPECIFICATIONS</b> (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
Static					
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	2.3	-	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 11 \text{ A}$	0.15	0.15	Ω
Forward Transconductance	g <sub>fs</sub>	$V_{DS} = 8 V, I_D = 5 A$	6	6.4	S
Dynamic					
Input Capacitance	C <sub>iss</sub>	$V_{DS}$ = 100 V, $V_{GS}$ = 0 V, f = 1 MHz	2222	1920	pF
Output Capacitance	Coss		208	90	
Reverse Transfer Capacitance	C <sub>rss</sub>		16	6	
Total Gate Charge	Qg	$V_{DS}$ = 480 V, $V_{GS}$ = 10 V, $I_{D}$ = 11 A	57	57	nC
Gate-Source Charge	Q <sub>gs</sub>		14	14	
Gate-Drain Charge	Q <sub>gd</sub>		26	26	
Drain-Source Body Diode Characteristics					
Diode Forward Voltage	V <sub>SD</sub>	$T_J$ = 25 °C, $I_S$ = 11 A, $V_{GS}$ = 0 V	0.83	-	V
Reverse Recovery Time	t <sub>rr</sub>	$T_J = 25 \text{ °C}, I_F = I_S = 11 \text{ A}, $ dI/dt = 100 A/µs, V <sub>R</sub> = 25 V	340	344	ns
Reverse Recovery Charge	Q <sub>rr</sub>		5.6	5.3	μC

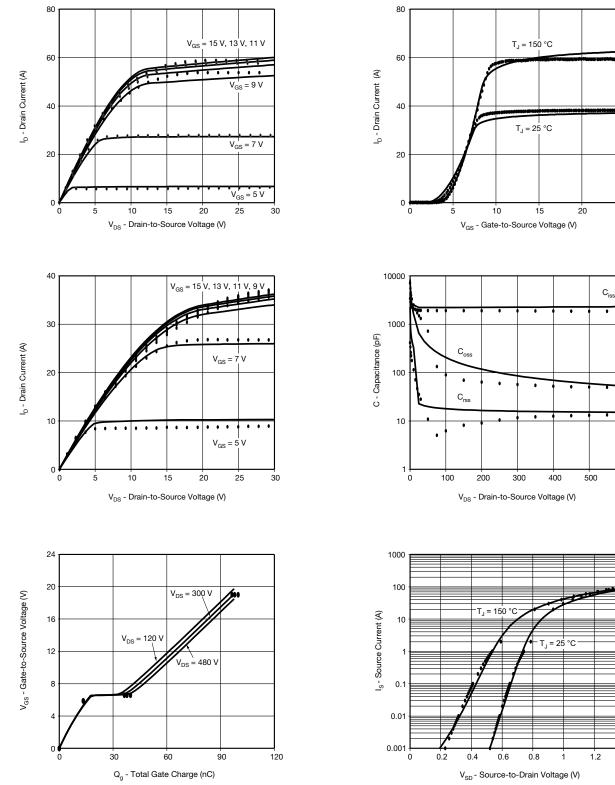


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25

600

### COMPARISON OF MODEL WITH MEASURED DATA (T<sub>J</sub> = 25 °C, unless otherwise noted)



#### Note

• Dots and squares represent measured data. Copyright: Vishay Intertechnology, Inc.

S16-1667-Rev. B, 29-Aug-16

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Document Number: 90822

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