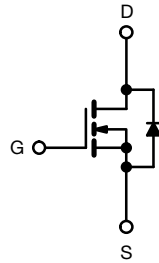
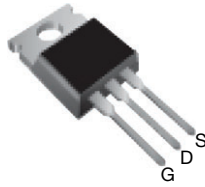


# Power MOSFET

**TO-220AB**


N-Channel MOSFET

## FEATURES

- Low gate charge  $Q_g$  results in simple drive requirement
- Improved gate, avalanche, and dynamic  $dV/dt$  ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Low  $R_{DS(on)}$
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS\***  
Available

## Note

\* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

## APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching
- Hard switched and high frequency circuits

## PRODUCT SUMMARY

$V_{DS}$ (V)	500	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.26
$Q_g$ max. (nC)	120	
$Q_{gs}$ (nC)	34	
$Q_{gd}$ (nC)	54	
Configuration	Single	

## ORDERING INFORMATION

Package	TO-220
Lead (Pb)-free	IRFB18N50KPbF

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	500	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current	$V_{GS} \text{ at } 10\text{ V}$	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current <sup>a</sup>	$I_{DM}$	68	
Linear derating factor		1.8	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	370	mJ
Repetitive avalanche current <sup>a</sup>	$I_{AR}$	17	A
Repetitive avalanche energy <sup>a</sup>	$E_{AR}$	22	mJ
Maximum power dissipation	$P_D$	220	W
Peak diode recovery $dV/dt$ <sup>c</sup>	$dV/dt$	7.8	V/ns
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
Soldering recommendations (peak temperature) <sup>d</sup>	For 10 s	300	
Mounting torque	6-32 or M3 screw	10	N

## Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 2.5\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 17\text{ A}$
- $I_{SD} \leq 17\text{ A}$ ,  $dI/dt \leq 376\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient <sup>a</sup>	R <sub>thJA</sub>	-	58	°C/W
Case-to-sink, flat, greased surface	R <sub>thCS</sub>	0.50	-	
Maximum junction-to-case (drain) <sup>a</sup>	R <sub>thJC</sub>	-	0.56	

**Note**

a. R<sub>th</sub> is measured at T<sub>J</sub> approximately 90 °C

**SPECIFICATIONS** (T<sub>J</sub> = 25 °C, unless otherwise noted)

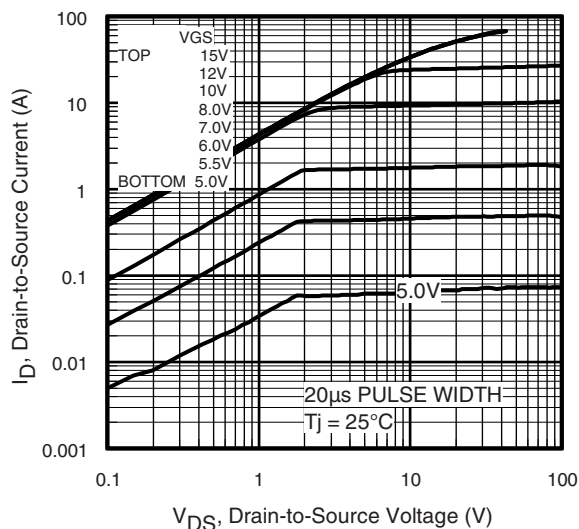
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	500	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA	-	0.59	-	V/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	-	5.0	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 30 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V	-	-	50	μA
		V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	250	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A <sup>b</sup>	-	0.26	0.29	Ω
Forward transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 10 A	6.4	-	-	S
<b>Dynamic</b>						
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5	-	2830	-	pF
Output capacitance	C <sub>oss</sub>		-	330	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	38	-	
Output capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 1.0 V, f = 1.0 MHz	-	3310	
Effective output capacitance	C <sub>oss eff.</sub>		V <sub>DS</sub> = 400 V, f = 1.0 MHz	-	93	nC
Total gate charge	Q <sub>g</sub>		V <sub>DS</sub> = 0 V to 400 V <sup>c</sup>	-	155	
Gate-source charge	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 17 A, V <sub>DS</sub> = 400 V, see fig. 6 and 13 <sup>b</sup>	-	-	ns
Gate-drain charge	Q <sub>gd</sub>			-	-	
Turn-on delay time	t <sub>d(on)</sub>			-	22	
Rise time	t <sub>r</sub>		V <sub>DD</sub> = 250 V, I <sub>D</sub> = 17 A, R <sub>G</sub> = 7.5 Ω, see fig. 10 <sup>b</sup>	-	60	ns
Turn-off delay time	t <sub>d(off)</sub>			-	45	
Fall time	t <sub>f</sub>			-	30	
Gate input resistance	R <sub>g</sub>	f = 1 MHz, open drain	0.7	-	2.7	Ω
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode	-	-	17	A
Pulsed diode forward current <sup>a</sup>	I <sub>SM</sub>		-	-	68	
Body diode voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 17 A, V <sub>GS</sub> = 0 V <sup>b</sup>	-	-	1.5	V
Body diode reverse recovery time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 17 A, dI/dt = 100 A/μs <sup>b</sup>	-	520	780	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	5.3	8.0	μC
Forward turn-on time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )				

**Notes**

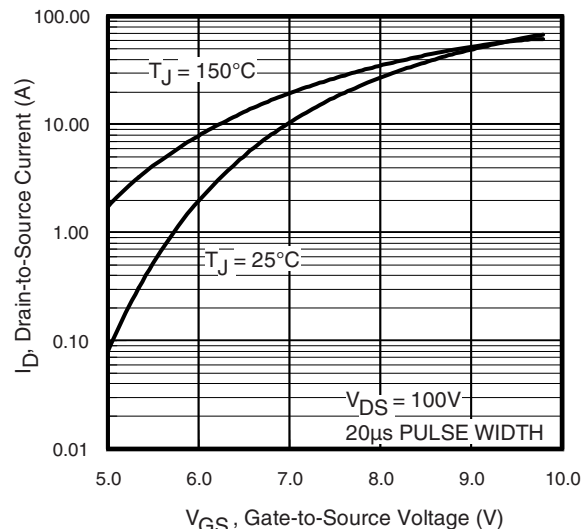
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)  
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %  
c. C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 % to 80 % V<sub>DS</sub>



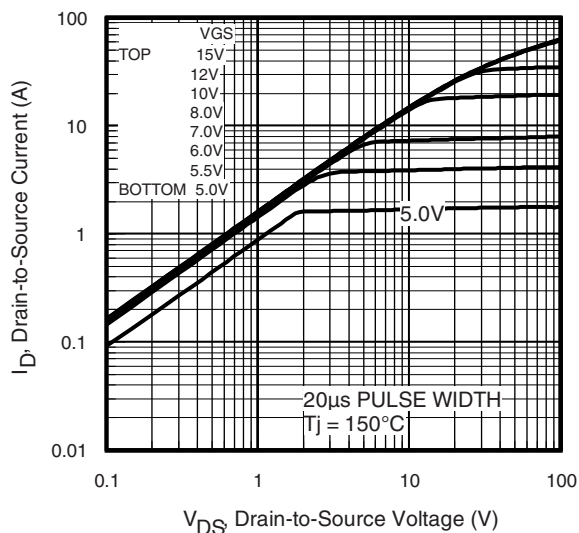
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



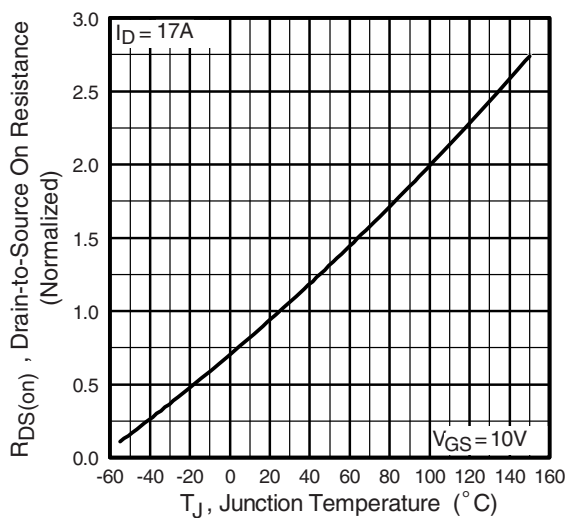
**Fig. 1 - Typical Output Characteristics**



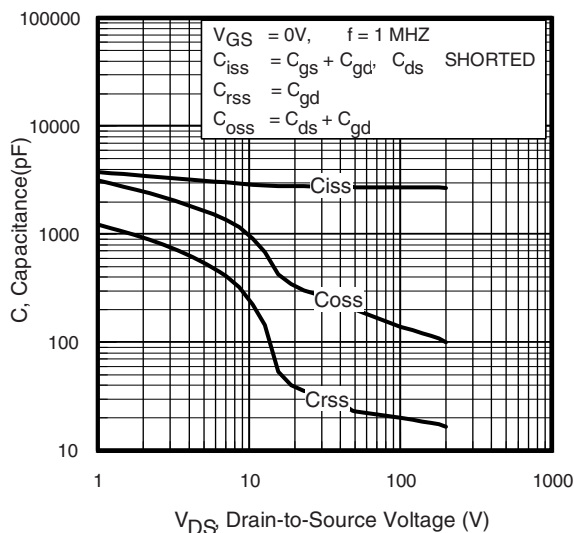
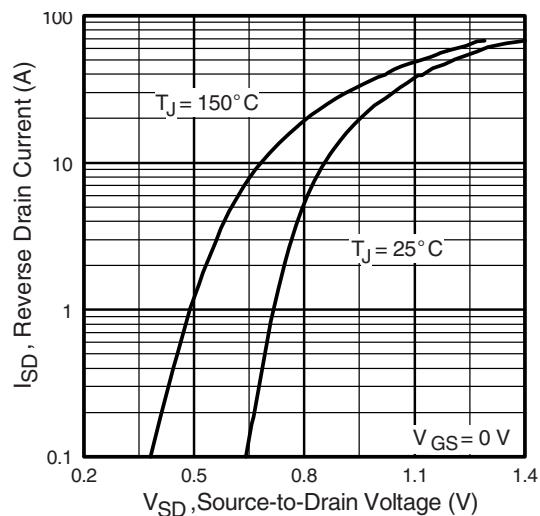
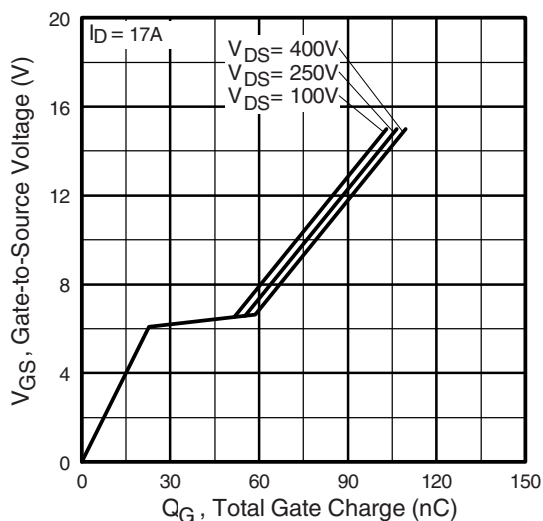
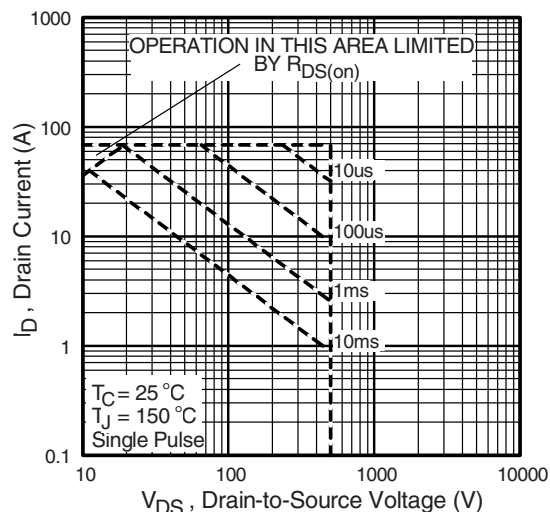
**Fig. 3 - Typical Transfer Characteristics**

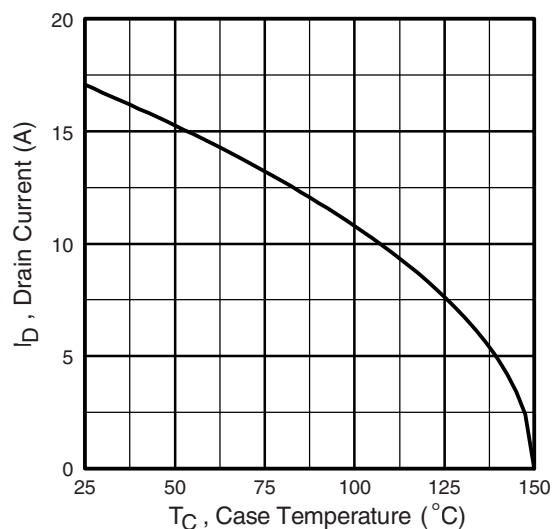
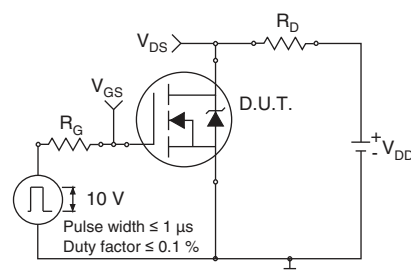


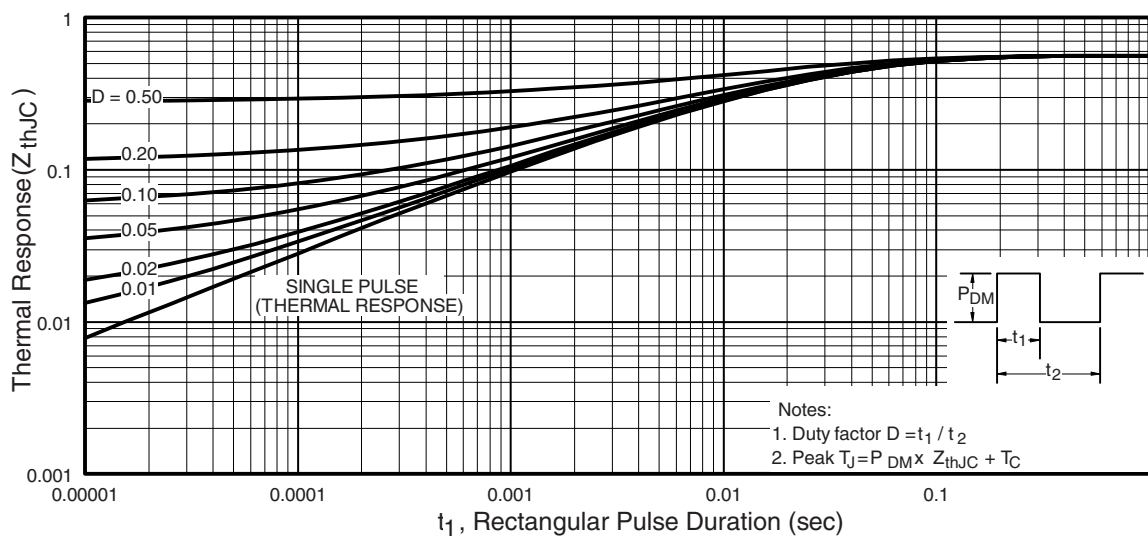
**Fig. 2 - Typical Output Characteristics**

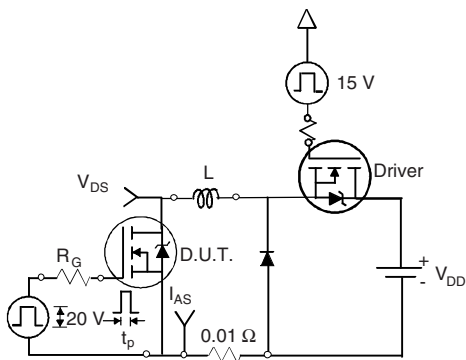
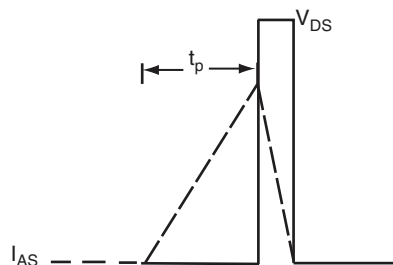
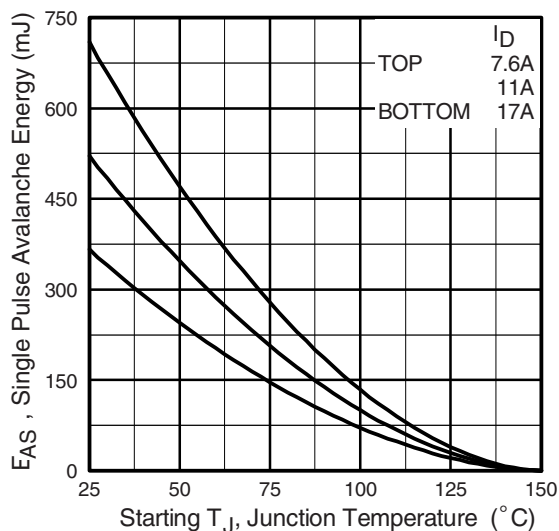
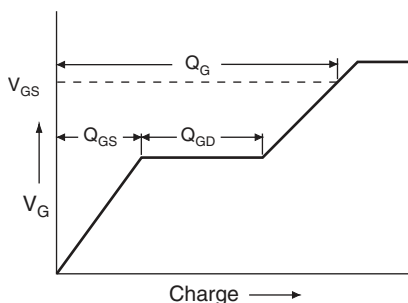
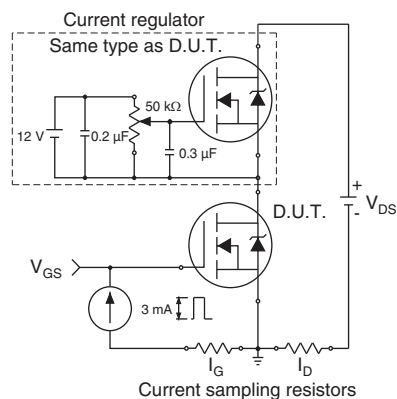


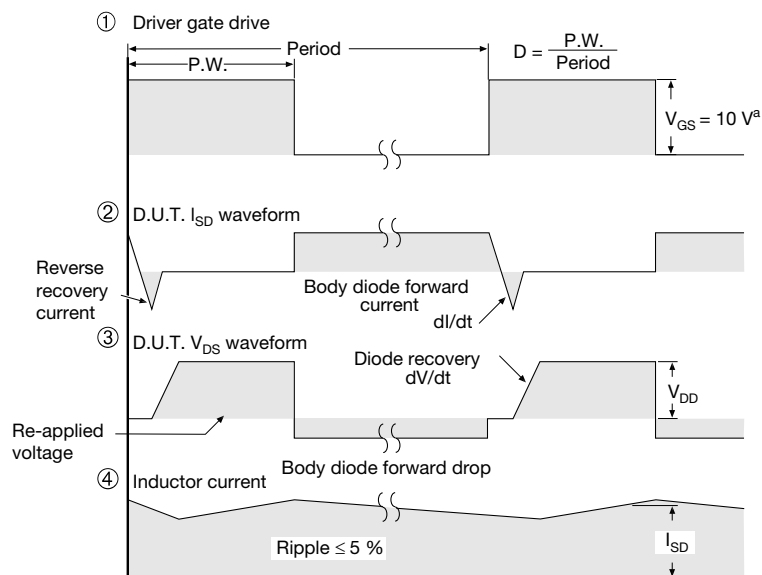
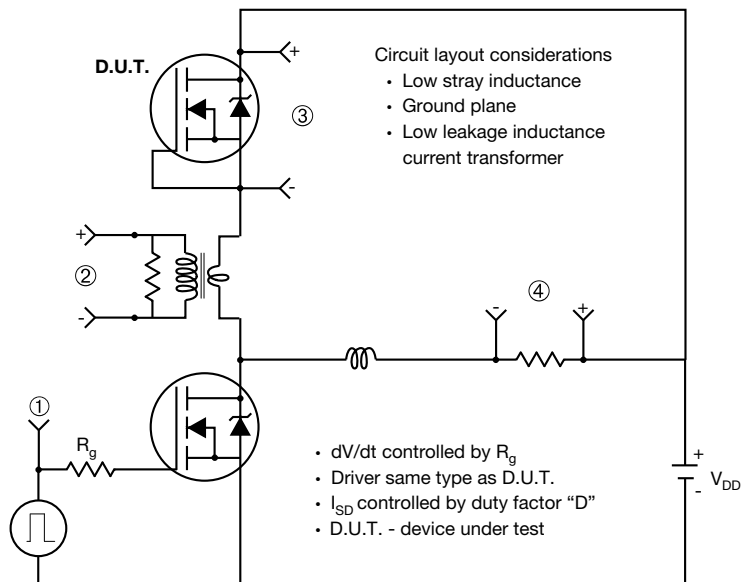
**Fig. 4 - Normalized On-Resistance vs. Temperature**


**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 8 - Maximum Safe Operating Area**


**Fig. 9 - Maximum Drain Current vs. Case Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**


**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

**Fig. 13a - Basic Gate Charge Waveform**

**Fig. 13b - Gate Charge Test Circuit**

**Peak Diode Recovery dV/dt Test Circuit**

**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

**Fig. 14 - For N-Channel**

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